

PCB BOARD SIZE
4 Layers
240mmX 240mm

Serena
PROJECT CODE:
PCB Version: SB
PCB Number: 10068

On Board Header

CONN	Default	DESCRIPTION
MFG1	1-X	FOR AUD_LINK_SDO_R_ENABLE AND FLASH
CLR_CMOS1	1-2	Reset CMOS data (Debug Only)
RCY1	1-X	BIOS RECOVERY MODE (Debug Only)
SCR1		Internal 2x5 USB header
WLKB1		Internal 2x6 USB header
CPUFAN1		1X4 pin CPU FAN
SYSFAN1		1X3 pin System FAN(On Riser)
PSUFAN1/2		1X4 and 1X3 pin PSU FAN
FP2		2X10 Front Panel Header
PWR1		2X12 ATX POWER CONN
APS1		2X5 APS Switch Board header (Debug Only)
LPC1		2X7 LPC debug port header (Debug Only)
SPD1		1X2 pin SPDIF header

XTAL Description

XTAL	Function	FJ Requirement	Spec	Capacitance
X1	PCH	None	+20ppm CL:18P	C1=C2=27pF
X2	USB3.0	+-100ppm	+20ppm CL:12P	C1=C2=33pF
X3	Clock	+-50ppm	+20ppm CL:16P	C1=22pF C2=27pF
X4	RTC	+-20ppm	+10ppm CL:12.5P	C1=C2=18pF
X5	LAN	+-30ppm	+20ppm CL:18P	C1=C2=33pF
X6	RLAN	+-30ppm	+20ppm CL:18P	C1=C2=33pF

Can't use FUJICOM

IQS/OSTOR
Citizen Miyota
Hermony (HELE)

SA BUILD

Cougar Point : Pre-ES2 B0 STEEPING QM2P
Cougar Point : TBD
Cougar Point : TBD

Intel LAN : WG82579LM QMWM MM#908148 A2 71.82579.B03
LAN : RTL8111E-VB-GRT 71.08111.I03

SIO : IT8728F 71.08728.00E

BOM Configuration
OS-CON/4+1 PHASE: (O)
EL/3+1 PHASE: (C)
USB3.0: (S)
INTEL LAN : (I)
REALTEK LAN: (K)
GRAPHICS SUPPORT: (D)
Unmount: (R)

W/Realtek: C, S, K, D
W/Intel: O, S, I, D

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09	Clock GEN - CK505
10	CPU LGA 1155-1
11	CPU LGA 1155-2
12	CPU LGA 1155-3
13	CPU LGA 1155-4
14	XDP/80 Port Header
15	DDR3 CHA DIMM 0
16	DDR3 CHA DIMM 1
17	DDR3 CHB DIMM 0
18	DDR3 CHB DIMM 1
19	PCH-Audio/GPIO/SPI
20	PCH-CLK/FDI/ONFI
21	PCH-SATA/FAN/DP
22	PCH-PCI/PCIE/DMI/USB
23	PCH-GND/Straps
24	PCH-Power
25	PCIEX16 CONNECTOR
26	PCIEX1 CONNECTOR
27	VGA Port
28	HDMI Port
29	SATA Port
30	Front USB
31	Rear USB+RJ45
32	INTEL Gb LAN 82579
33	Realtek Gb LAN-RTL8111E
34	Audio Codec-ALC662
35	Audio CODOC JACKS
36	USB3.0 SIS100
37	USB3.0 POWER
38	EMI
39	DSW
40	Super I/O ITE8728
41	TBD
42	CPU FAN / SYS FAN Header
43	AMT/KBMS
44	SW LED / Front Panel
45	ATX POWER/MT Hole
46	Dual Power
47	SYSTEM POWER
48	DDR POWER
49	CPU VTT&CPU_SA
50	VRM CONTROLLER L6758A
51	VRM OUTPUT&GPU OUTPUT

PCB BOARD SIZE
244mmX 244mm
4 Layer

Internal Slot/Header
Front/Rear IO
Chipset

VRM 12
(3+1Phase 95W)
(4+1Phase 130W?)

PCI_E_X16

PCI EXPRESS Gen2

INTEL
Sandy Bridge
SOCKET FCLGA LGA1155
(95W)
37.5X37.5mm

Sandy Bridge
LGA 1155

Channel A
64 bit
1066/1333MHZ

Channel B
64 bit
1066/1333MHZ

DDR3 DIMM
Unbuffered 4GB

DDR3 DIMM
Unbuffered 4GB

7MHz
100MHz

FDI
DMI
PCI

D-SUB PORT

RGB

HDMI PORT

Port D

USB2.0X2 FRONT HEADER

USB 2.0 *10

480Mb/s

USB2.0X2 FRONT HEADER

SPIFlash ROM

64/32M/16M

USB 2.0 x4 REAR

USB 2.0 x2 REAR(with RJ45)

INTEL PCH
COUGER POINT
H67 P67

PCI Express Interface

PCI_E_X1

PCI Express Interface

PCI_E_X1

PCI Express Interface

PCI_E_X1

PCI Express Interface*2

USB3.0 controller
SIS100

USB3.0 X2 REAR

25M

Intel LAN
82579LM

25M

Option
Realtek LAN
8111E

25M

RJ45

120MHz
100MHz
96MHz
48MHz
33MHz
14.318MHz
32.768KHz

32.7K

PCPGA 989PIN
27x27mm

Cougar Point

LPC BUS

SIO ITE8728

QST

CPU 1X4 FAN

PS/2 KB

PS/2 Mouse

SYS 1X3 FAN

SATA 3.0
(Port 1)

SATA 3.0
(Port 0)

SATA3.0 BUS

SATA 2.0
(Port 3)

SATA 2.0
(Port 2)

SATA2.0 BUS

SATA 2.0
(Port 5)

SATA 2.0
(Port 4)

SATA2.0 BUS

REAR Line - IN

REAR Line - Out

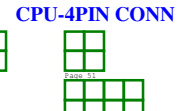
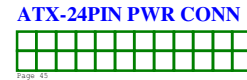
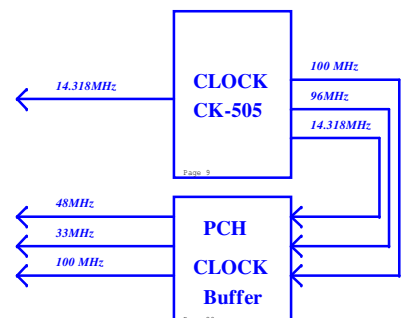
REAR MIC -IN

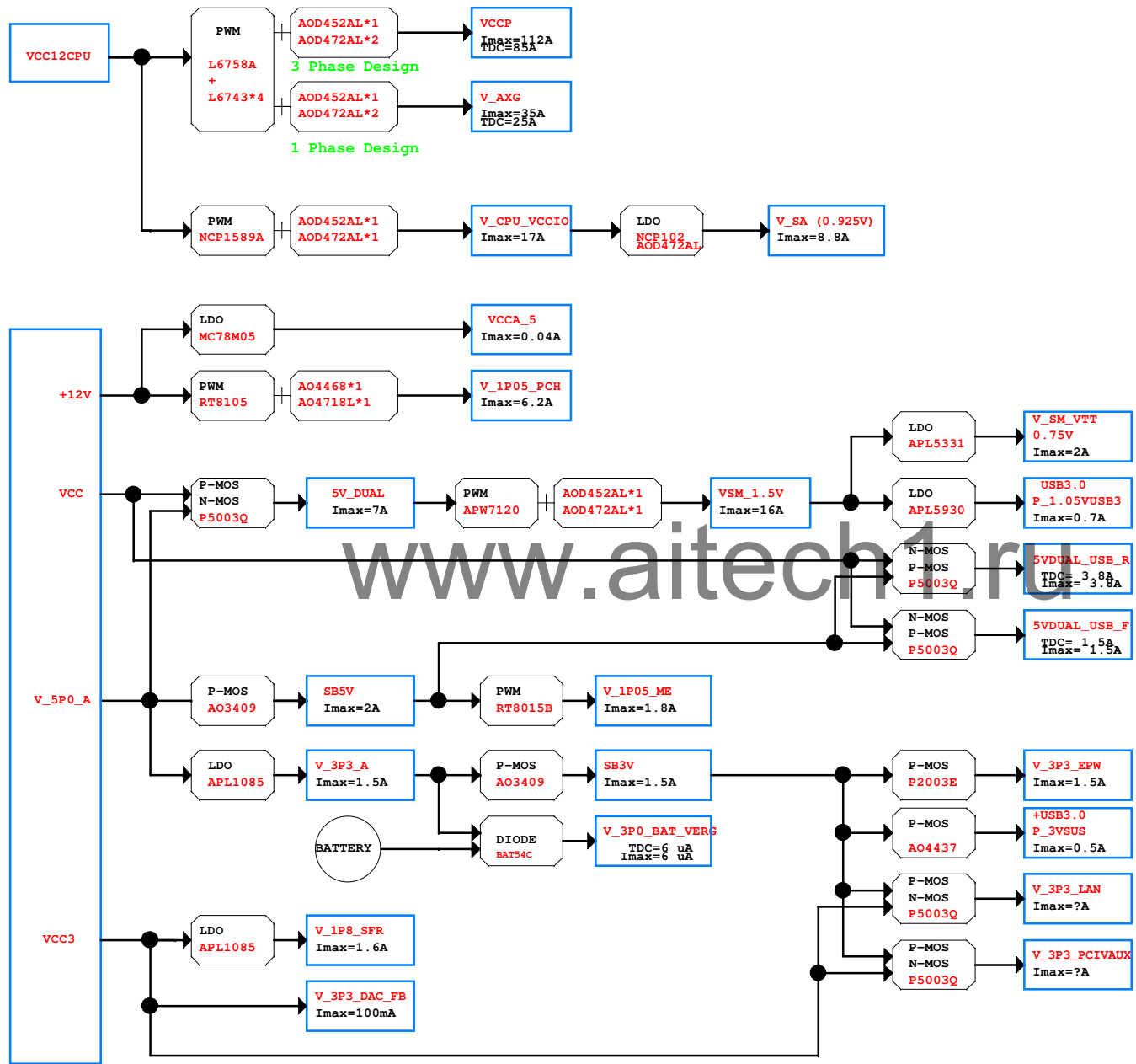
FRONT MIC -IN

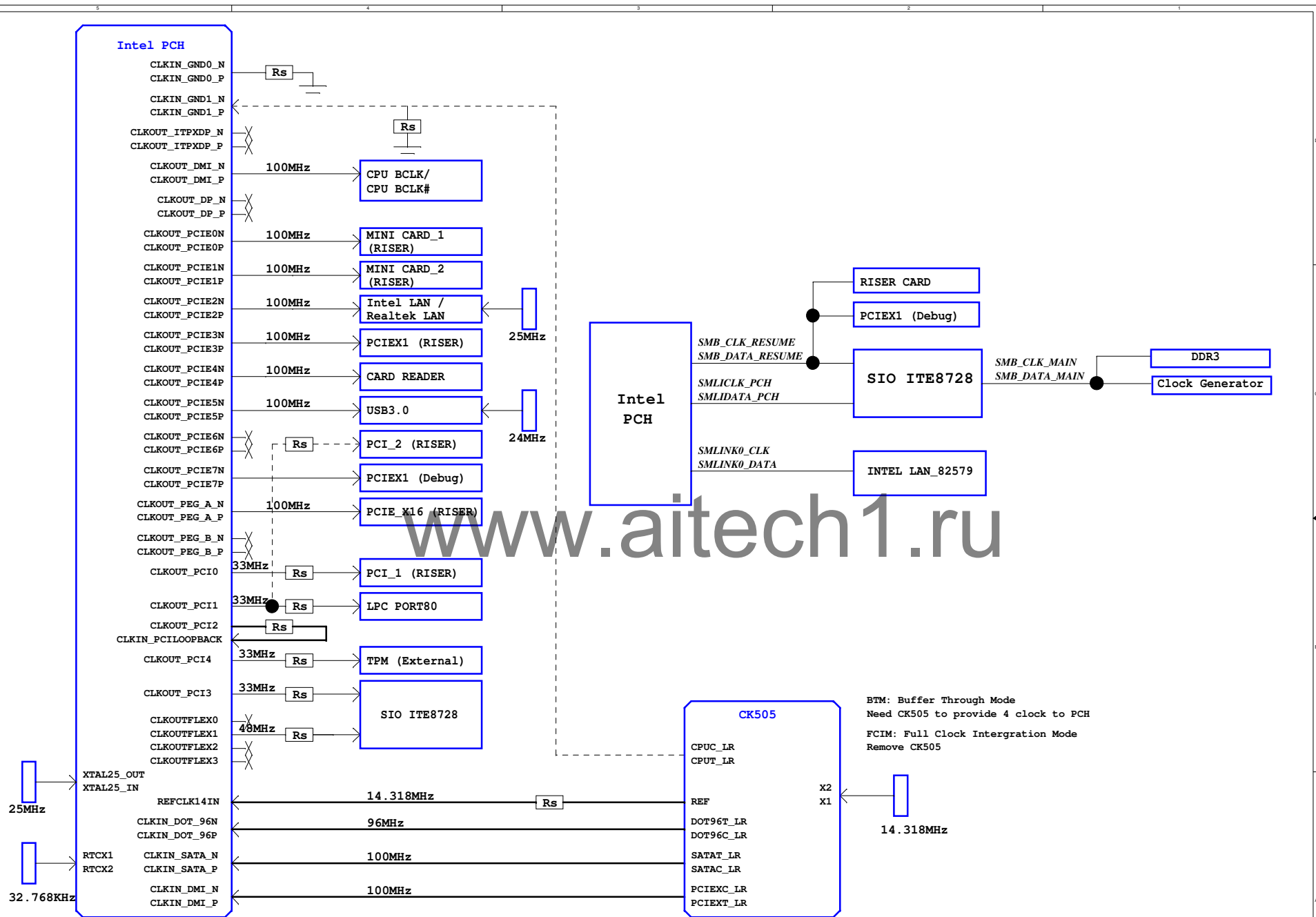
FRONT HP - OUT

HDA CODEC
ALC662

High Definition Audio

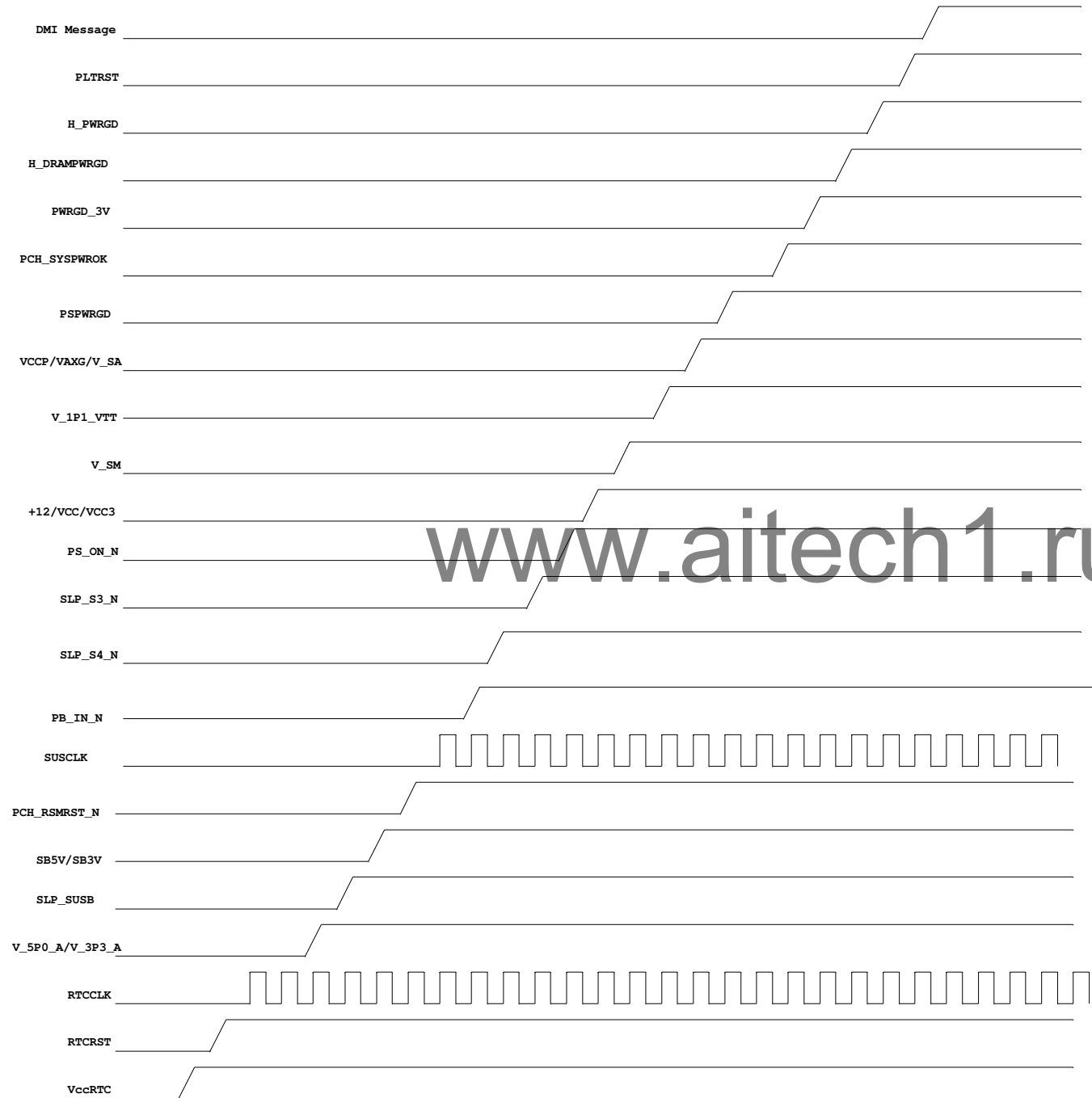


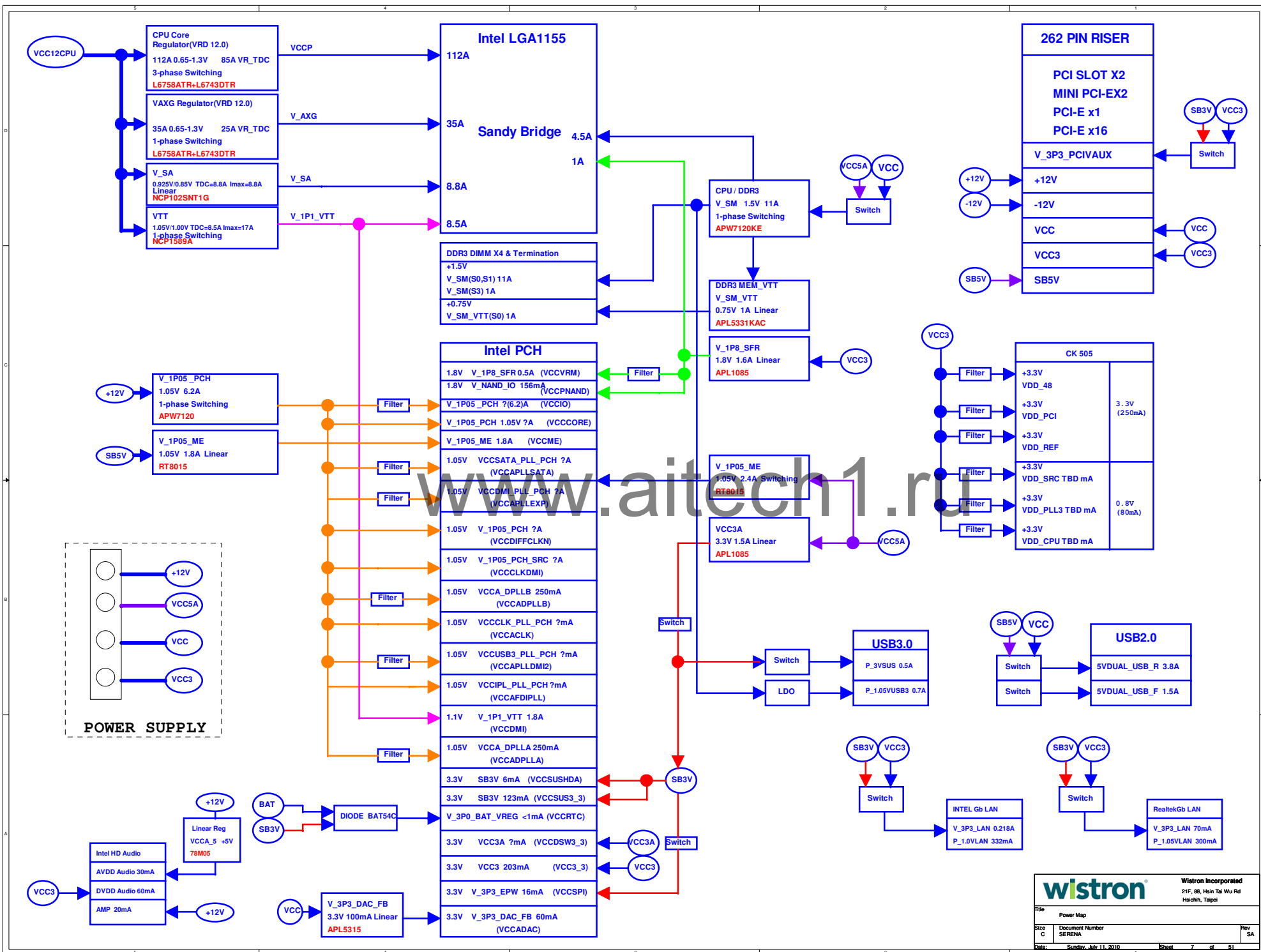




Note: is Reserve
Note: Rs is series resistor

POWER ON SEQUENCE





TBD
www.aitech1.ru

PCH CLOCK

22 CK_98M_DREF_DP <<
 22 CK_98M_DREF_DN <<
 21 CK_SATA_PCH_DP <<
 21 CK_SATA_PCH_DN <<
 22 100M_DMI_PCH_DP <<
 22 100M_DMI_PCH_DN <<
 20 CK_100M_CPHY_PCH_LN_DP <<
 20 CK_100M_CPHY_PCH_LN_DN <<

14M CLOCK

20 CK_14M_PCH <<

OTHERS

14,15,16,17,18,40 SMB_DATA_MAIN <<
 14,15,16,17,18,40 SMB_CLK_MAIN <<
 14,19,50 VR_READY <<
 14,19,40,45,46,47,49 SUP_50_N <<

0827 remove

Stuff for FCIM mode

CK_98M_DREF_DP R12 1 10KRU3-3GP
 CK_98M_DREF_DN R13 1 10KRU3-3GP
 CK_SATA_PCH_DP R14 1 10KRU3-3GP
 CK_SATA_PCH_DN R16 1 10KRU3-3GP
 100M_DMI_PCH_DP R17 1 10KRU3-3GP
 100M_DMI_PCH_DN R18 1 10KRU3-3GP
 CK_14M_PCH R19 1 10KRU3-3GP

CLK input buffers on PCH that not driven from Q305 should be terminated properly using 10KRU3 input or differential input, 10K pull-up resistors.

www.aitech.com

Low threshold input FSC="1" voltage, MAX=1.5V

FREQ Select Table Default is 100MHz

FREQ	FSC	FSB	FSA	STUFF	EMPT
100	1	0	1	R420 R460 R466 R467	R431
133	0	0	1	R420 R460 R466	R431 R491

Different with CRB

CLOCK

20 CK_PE_100M_MCP_DN
20 CK_PE_100M_MCP_DP

CPU_SA

49 VCCSA_VDD
49 VCCSA_SENSE

CPU_VTT

49 VCCIO_SEL
49 VCCIO_SENSE
49 VSSIO_SENSE

CPU_AXG

50 VCCAXG_SENSE
50 VSSAXG_SENSE

CPU_VCORE

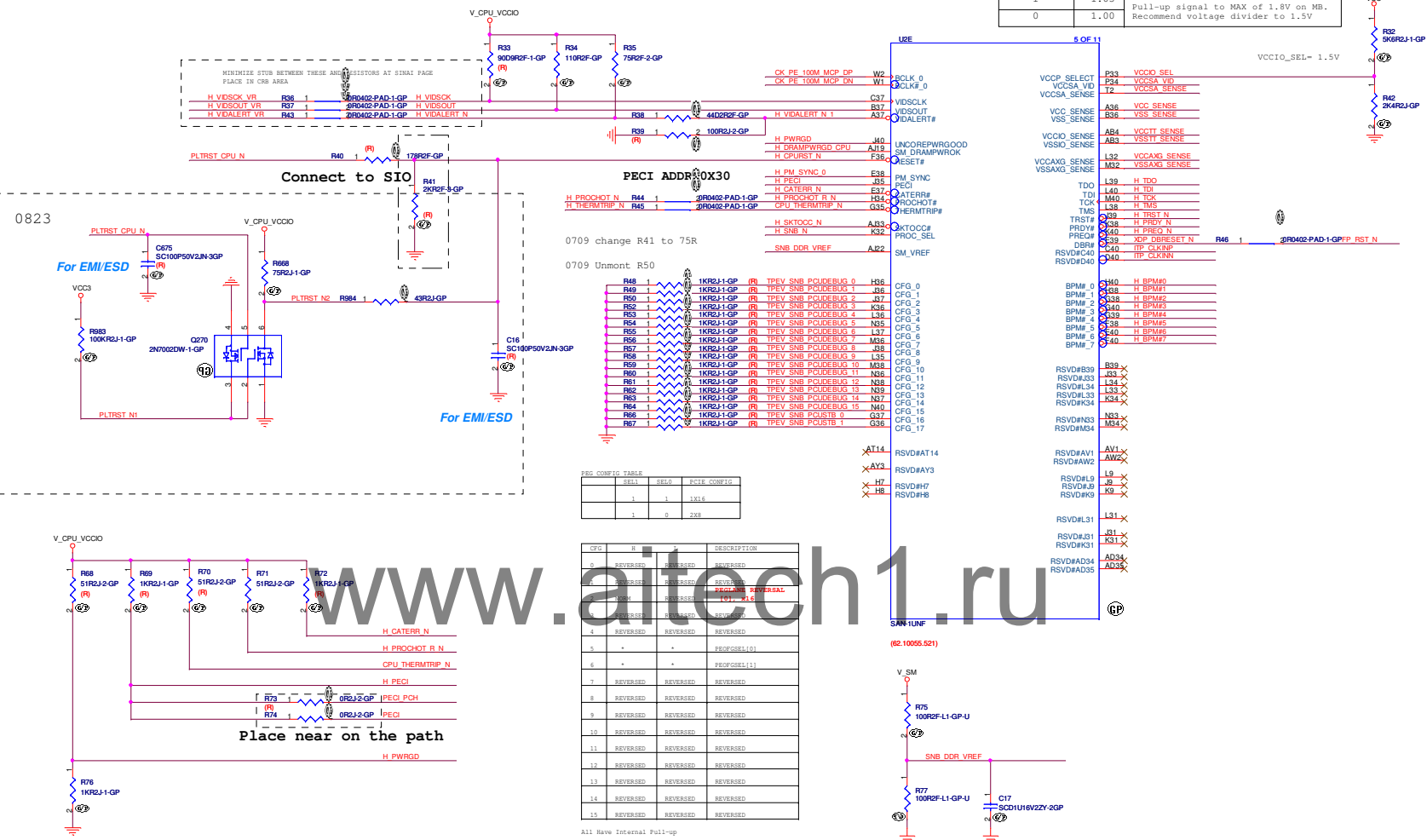
50 VCC_SENSE
50 VSS_SENSE

ITP

14 H_TDO
14 H_TDI
14 H_TCK
14 H_TMS
14 H_TRST_N
14 H_PRODY_N
14 H_PRODY_N
14 ITP_CLKIN_N
14 ITP_CLKIN_P
14 H_CPU_RST_N
14 H_BPM#0
14 H_BPM#1
14 H_BPM#2
14 H_BPM#3
14 H_BPM#4
14 H_BPM#5
14 H_BPM#6
14 H_BPM#7

OTHER

40 PLTRST_CPU_N
14,19 H_PWRGD
14,19,44 PP_RST_N
19 H_DRAMPWRGD_CPU
21 PECH_PCH
40 PECH
50 H_PROCHOT_N
21 H_PM_SYNC_0
19 H_SKTDOCC_N
23 H_SNB_N
14 TPEV_SNB_POUDBUG_0



FDI

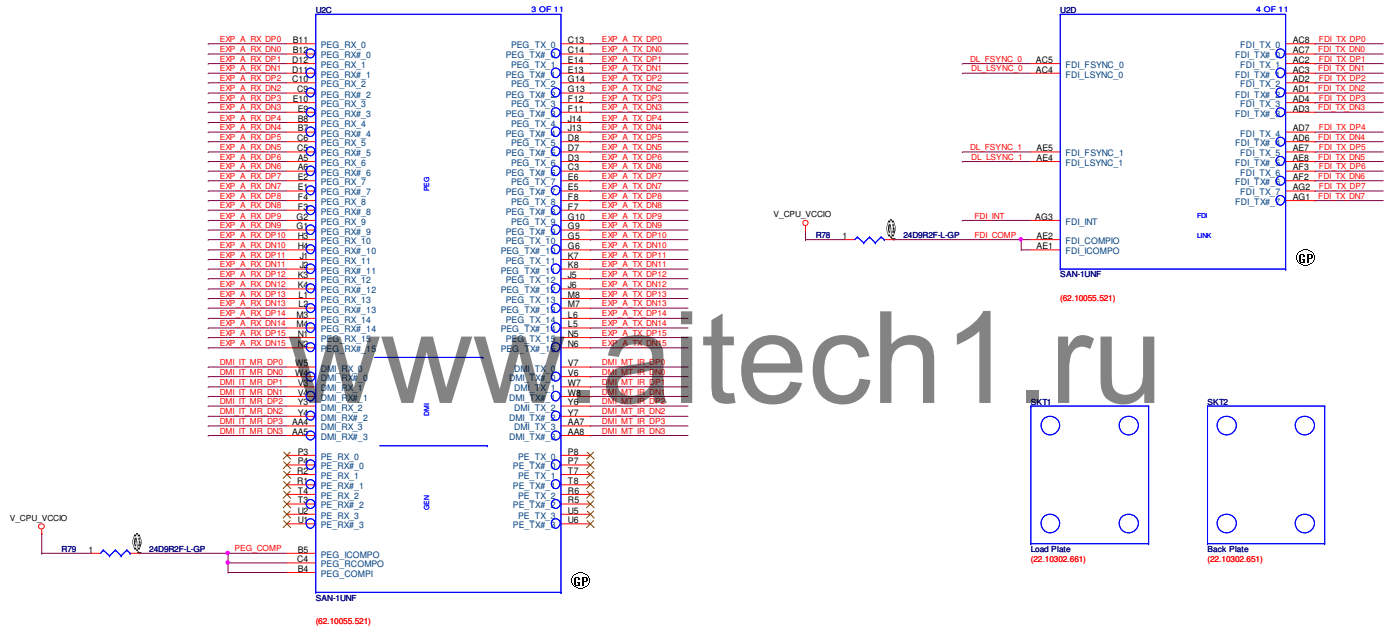
20 DL_FSYNC_0
20 DL_LSYNC_0
20 DL_FSYNC_1
20 DL_LSYNC_1
20 FDI_INT
20 FDI_TX_DP[0..7]
20 FDI_TX_DN[0..7]

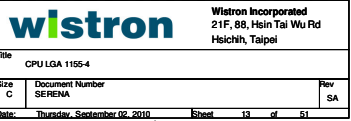
PCIEX16

25 EXP_A_TX_DP[0..15]
25 EXP_A_TX_DN[0..15]
25 EXP_A_RX_DP[0..15]
25 EXP_A_RX_DN[0..15]

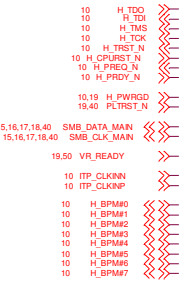
DMI

22 DMI_IT_MR_DP[0..3]
22 DMI_IT_MR_DN[0..3]
22 DMI_MT_IR_DP[0..3]
22 DMI_MT_IR_DN[0..3]

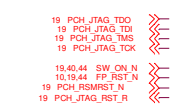




XDP (ITP) for CPU



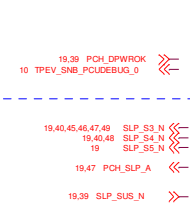
XDP (ITP) for PCH



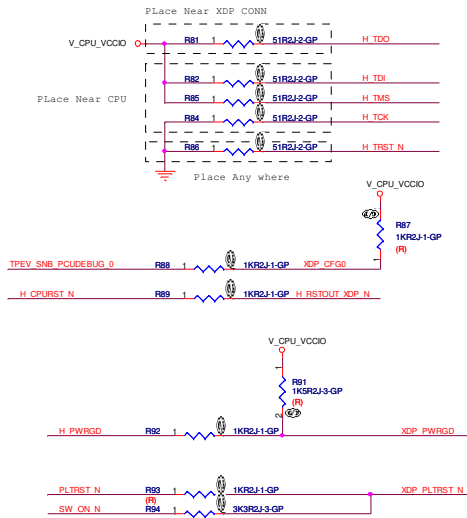
LPC DEBUG PORT



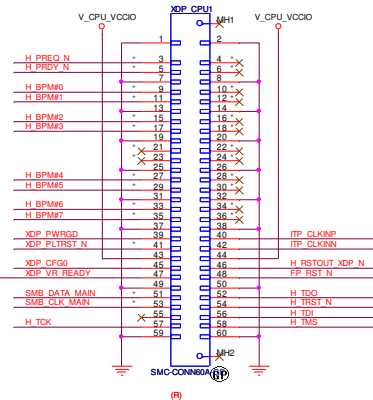
SBD HDR



XDP (ITP) for CPU

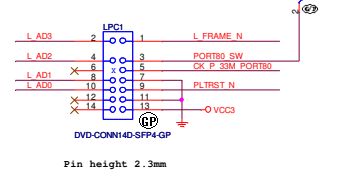


All parts can be placed at back side

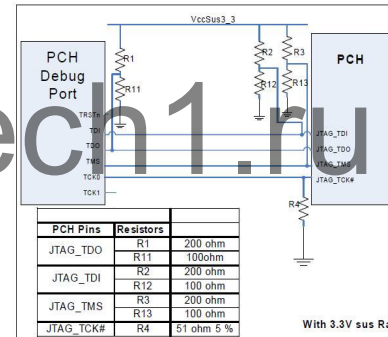
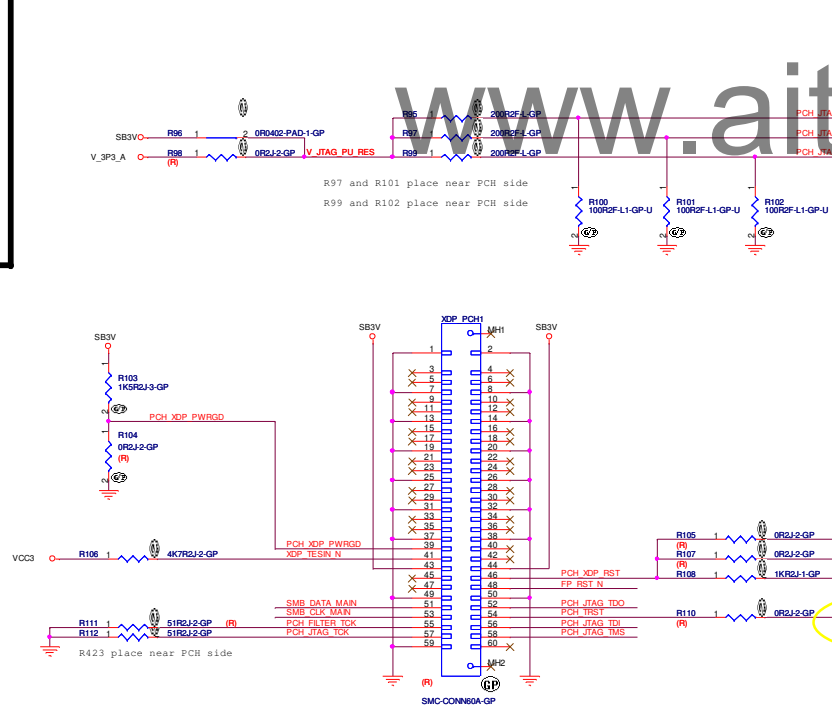


* : Optional signals

LPC DEBUG PORT



XDP (ITP) for PCH

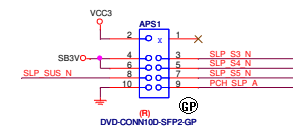


PCH Pins	Resistors	Value
JTAG_TDO	R1	200 ohm
JTAG_TDI	R2	200 ohm
JTAG_TMS	R3	200 ohm
JTAG_TCK#	R4	51 ohm 5%

With 3.3V sus Rail

PCH pins	Resistor	Value
PCH_JTAG_TDO	R432	200 ohm
PCH_JTAG_TDI	R433	100 ohm
PCH_JTAG_TMS	R426	200 ohm
PCH_JTAG_TCK	R427	100 ohm
PCH_JTAG_TMS	R418	200 ohm
PCH_JTAG_TCK	R419	100 ohm
PCH_JTAG_TCK	R423	51 ohm 5%

APS SBD PORT



Pin height 2.3mm

Mount for D and unmount after MP

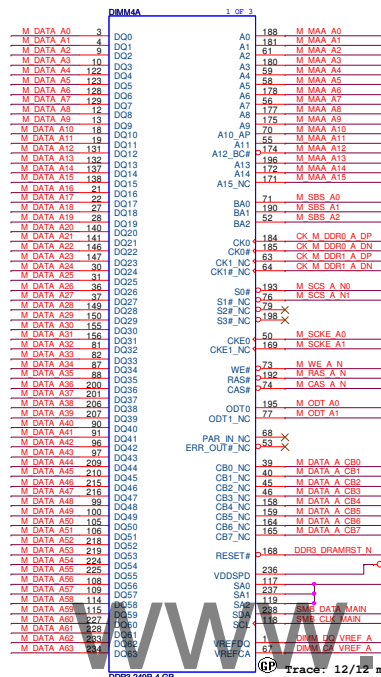
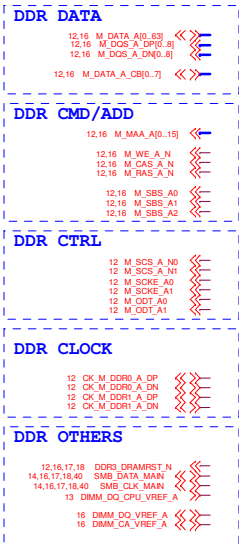
0713

All parts can be placed at back side

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Haichih, Taipei

File	XDP/BD PORT HEADER	Rev	SA
Size	Document Number		
C	SEIENA		
Date	Wednesday, September 01, 2010	Sheet	14 of 51



DDR DATA

12,15 M_DATA_A[0..63] <<>>
12,15 M_DQS_A_DP[0..8] <<>>
12,15 M_DQS_A_DN[0..8] <<>>

DDR CMD/ADD

12,15 M_MAA_A[0..15] <<>>
12,15 M_WE_A_N <<>>
12,15 M_CAS_A_N <<>>
12,15 M_RAS_A_N <<>>
12,15 M_SBS_A0 <<>>
12,15 M_SBS_A1 <<>>
12,15 M_SBS_A2 <<>>

DDR CTRL

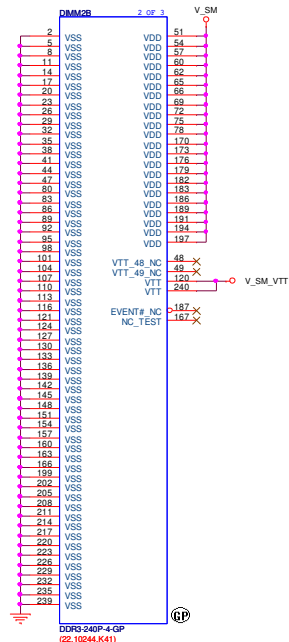
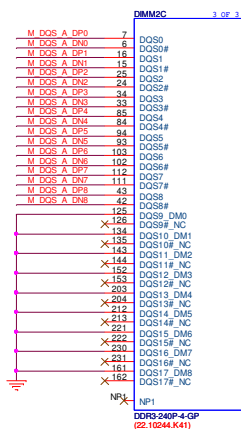
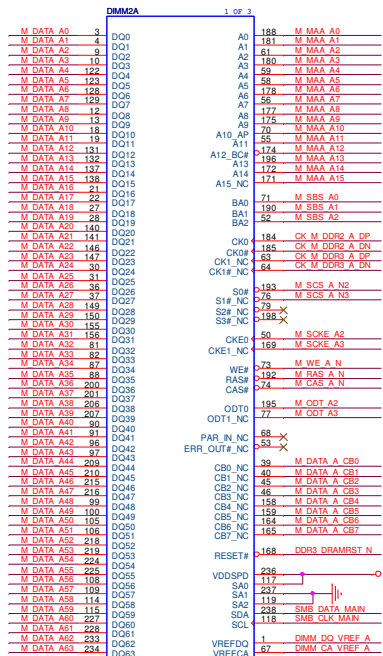
12 M_SCS_A_N2 <<>>
12 M_SCS_A_N3 <<>>
12 M_SCKE_A2 <<>>
12 M_SCKE_A3 <<>>
12 M_ODT_A2 <<>>
12 M_ODT_A3 <<>>

DDR CLOCK

12 CK_M_DDR2_A_DP <<>>
12 CK_M_DDR2_A_DN <<>>
12 CK_M_DDR3_A_DP <<>>
12 CK_M_DDR3_A_DN <<>>

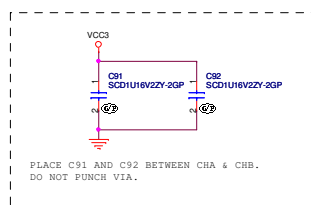
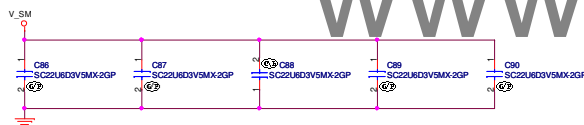
DDR OTHERS

12,15,17,18 DDR3_DRAMRST_N <<>>
14,15,17,18,40 SMB_DATA_MAIN <<>>
14,15,17,18,40 SMB_CLK_MAIN <<>>
15 DIMM_DQ_VREF_A <<>>
15 DIMM_CA_VREF_A <<>>



CHANNEL A DIMM1

CHA SMB ADDRESS: 001
CHA SPD R/W: 0'A3, 0'A2



PLACE C91 AND C92 BETWEEN CHA & CHB.
DO NOT PUNCH VIA.

www.aitech1.ru

Place Near Power Pin

Net	CAP	AMOUNT
V_SM	22uf 0603 X5R	5
V_SM_VTT	4.7uf 0603 X5R	1
V_SM_VTT	0.1uf 0402 Y5V	1

wlstron

Wistron Incorporated
21F, 88, Heintai Wu Rd
Hsichih, Taipei

Title: DDR3 CHA DIMM1
Size: C
Document Number: SERENA
Date: Friday, August 27, 2010
Sheet: 16 of 51

DDR DATA

12,17 M_DATA B[0..63] <<>>
12,17 M_DQS B_DP[0..63] <<>>
12,17 M_DQS B_DN[0..63] <<>>
12,17 M_DATA B_CB[0..7] <<>>

DDR CMD/ADD

12,17 M_MAA_B[0..15] <<>>

DDR CTRL

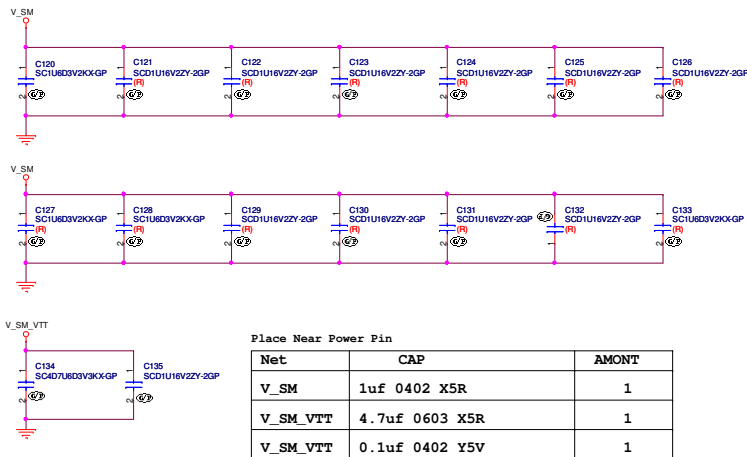
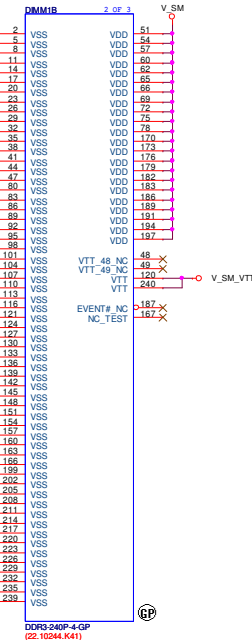
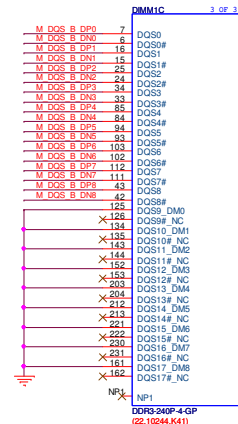
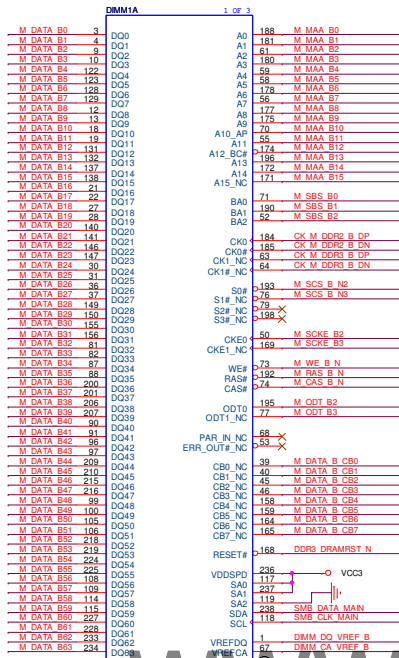
12 M_SCS_B_N2 <<>>
12 M_SCS_B_N3 <<>>
12 M_SCKE_B2 <<>>
12 M_SCKE_B3 <<>>
12 M_ODT_B2 <<>>
12 M_ODT_B3 <<>>

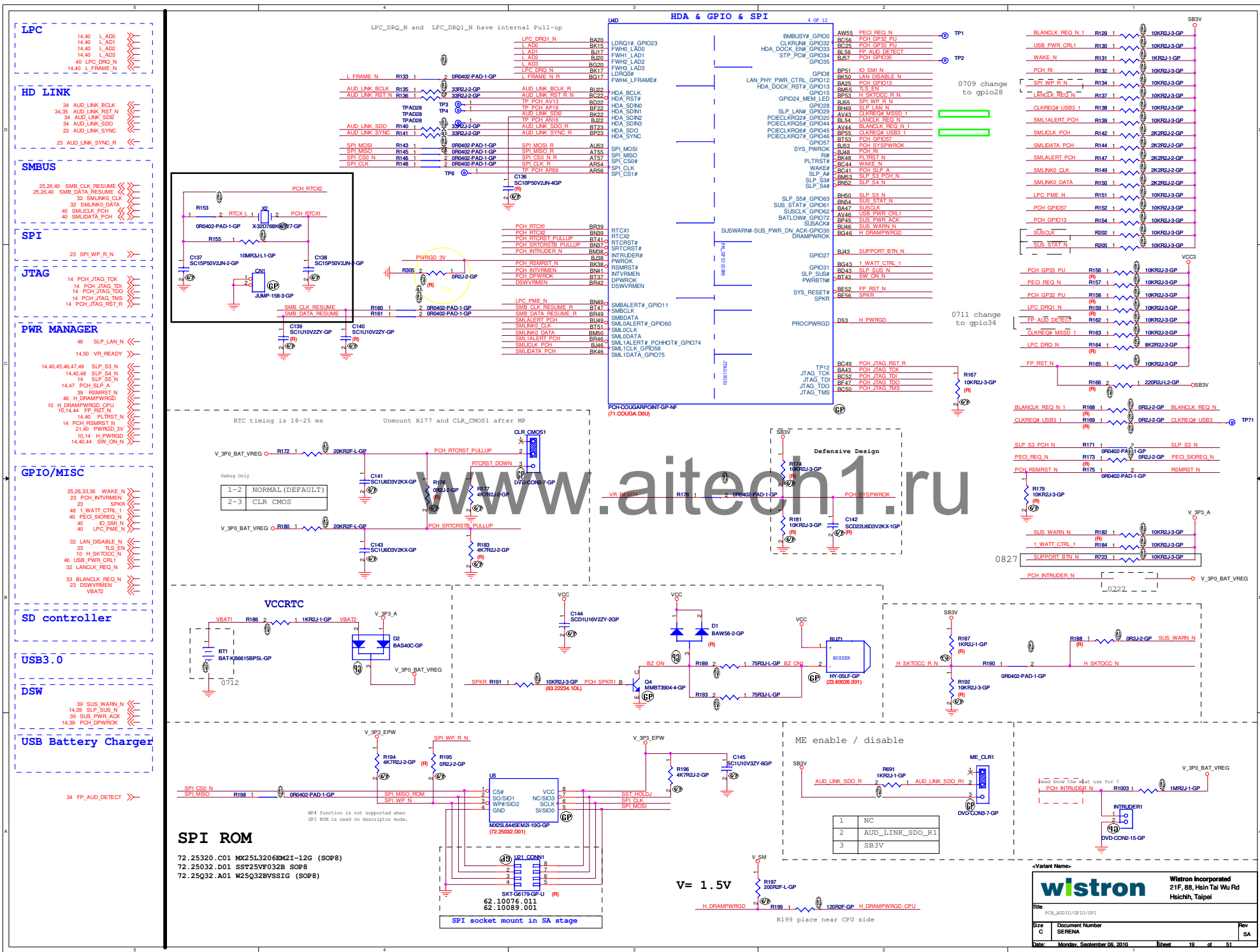
DDR CLOCK

12 CK_M_DDR2_B_DP <<>>
12 CK_M_DDR2_B_DN <<>>
12 CK_M_DDR3_B_DP <<>>
12 CK_M_DDR3_B_DN <<>>

DDR OTHERS

12,15,16,17 DDR3_DRAMRST_N <<>>
14,15,16,17,40 SMB_DATA_MAIN <<>>
14,15,16,17,40 SMB_CLK_MAIN <<>>
17 DIMM_DQ_VREF_B <<>>
17 DIMM_CA_VREF_B <<>>





SPI ROM

72.25320.C01 MX25L3206M2I-12G (SOP8)
72.25032.D01 SST25VF032B SOP8
72.25032.A01 W25Q32BVSSIG (SOP8)

SPI socket mount in SA stage

ME enable / disable

1	NC
2	AUD_LINK_SDO_R1
3	SB3V

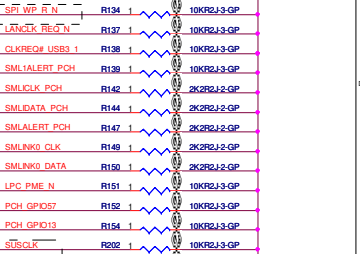
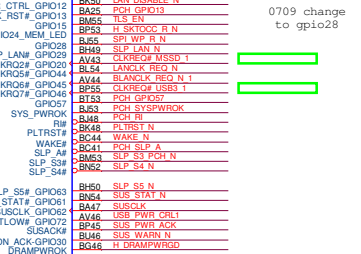
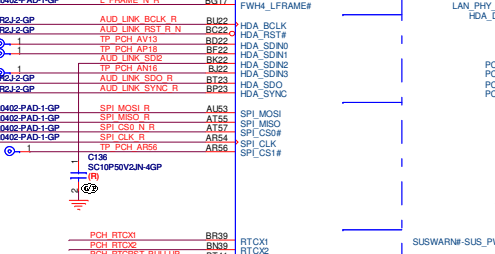
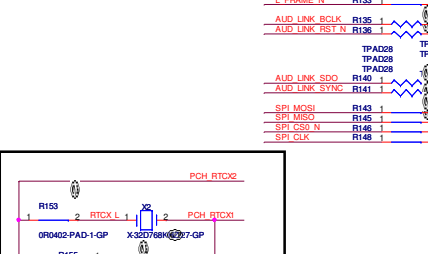
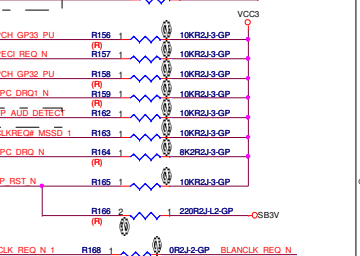
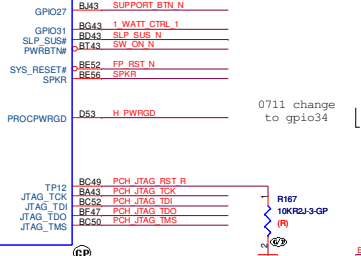
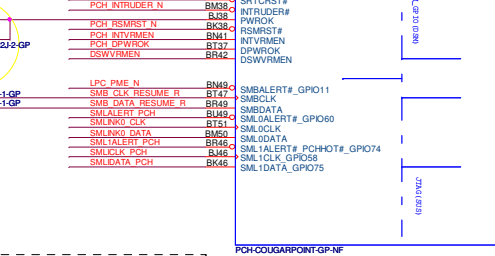
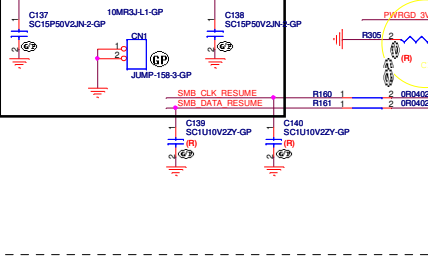
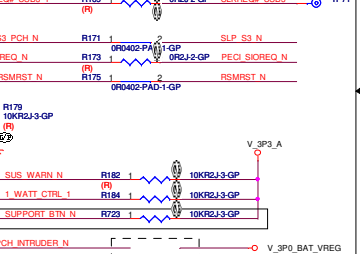
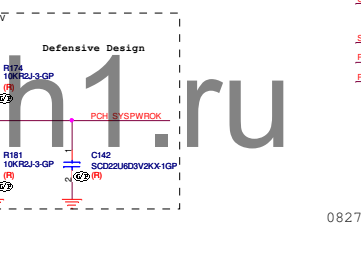
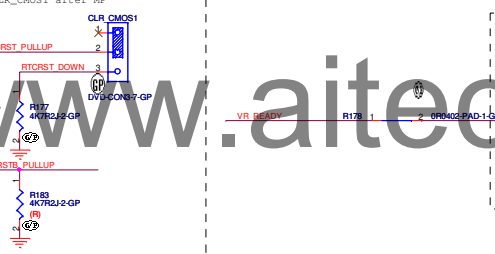
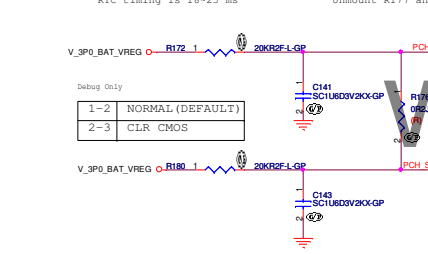
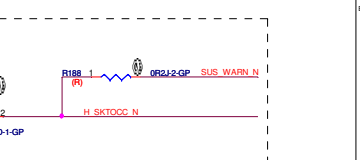
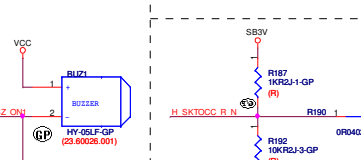
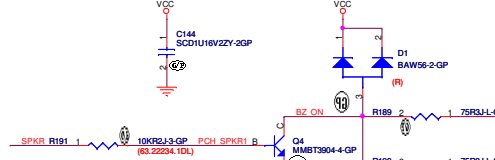
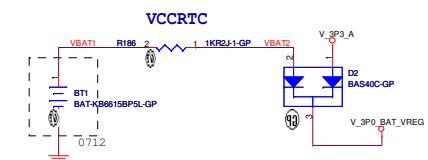
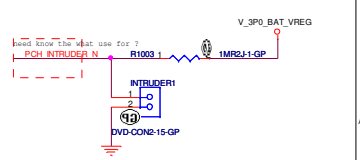
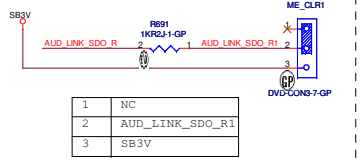
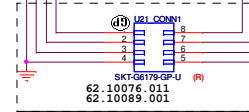


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21F, 88, Heintai Wu Rd
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File: PCH_ASD10/0210/SP1

Size	Document Number	Rev
C	SEIEMNA	SA

Date: Monday, September 08, 2010 Sheet 19 of 51



PCI CLOCK

```

40 CK_P_33M_SIO
22 CK_PCH_33M_FB
14 CK_P_33M_PORTB0

```

PCIE CLOCK

25 CK_PE_100M_16PORT_DP

25 CK_PE_100M_16PORT_DN

10 CK_PE_100M_MCP_DN

10 CK_PE_100M_MCP_DP

26 CK_PCIE1_1_DN

26 CK_PCIE1_1_DP

26 CK_PCIE1_3_DN

26 CK_PCIE1_3_DP

26 CK_PCIE1_2_DN

26 CK_PCIE1_2_DP

```

32 CK_GLAN_DN
32 CK_GLAN_DP
33 CK_BLAN_DN
33 CK_BLAN_DP

```

36 CLK_100_USB3_DN

14M CLOCK

9. CK 14M BCH

48M CLOCK

40 CLK_48M_SIO <<—

FDI

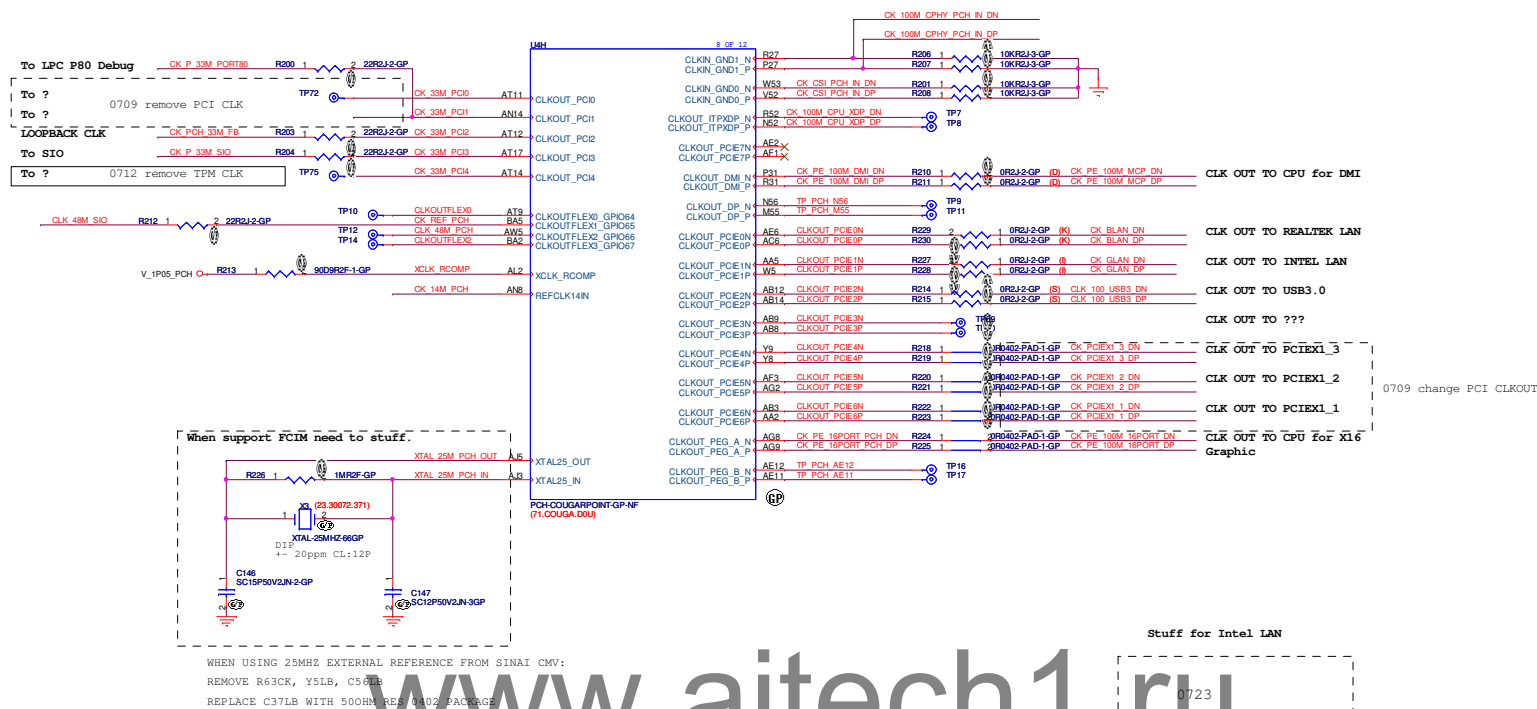
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11 FDI_TX_DN[0..7]
11 FDI_TX_DP[0..7]
11 DL_FSYNC_0
11 DL_LSYNC_0
11 DL_FSYNC_1
11 DL_LSYNC_1
11 FDI_INT

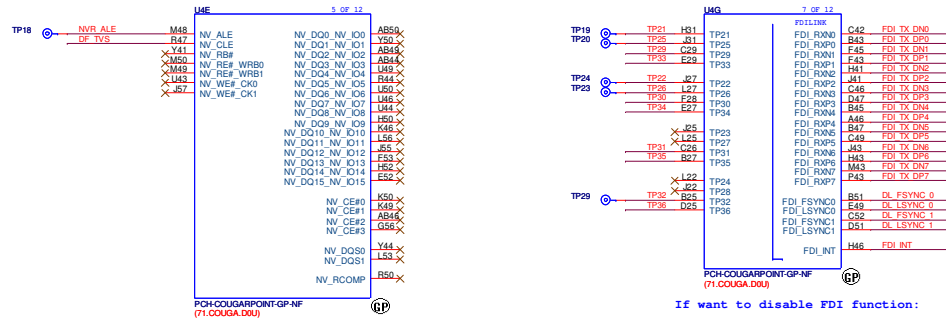
```

Others

23 DF_TV5 <<>>—



DUAL CHANNEL NAND INTERFACE



If want to disable FDI function:

- 1.Connect FDI_FSYNC and FDI_LSYNC and FDI_INT to GND
- 2.Float FDI TX and RX

<Variant Name>



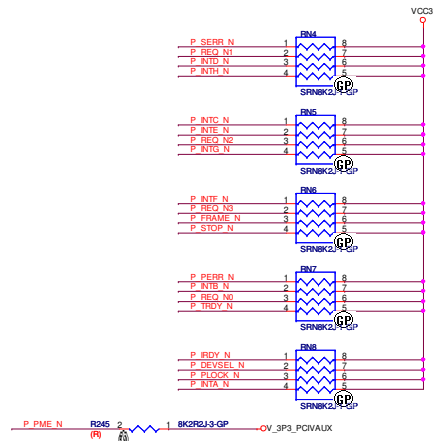
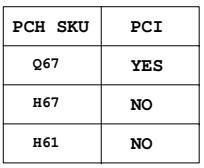
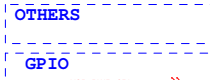
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	PCR_CLK/FDI/CNFI
-------	------------------

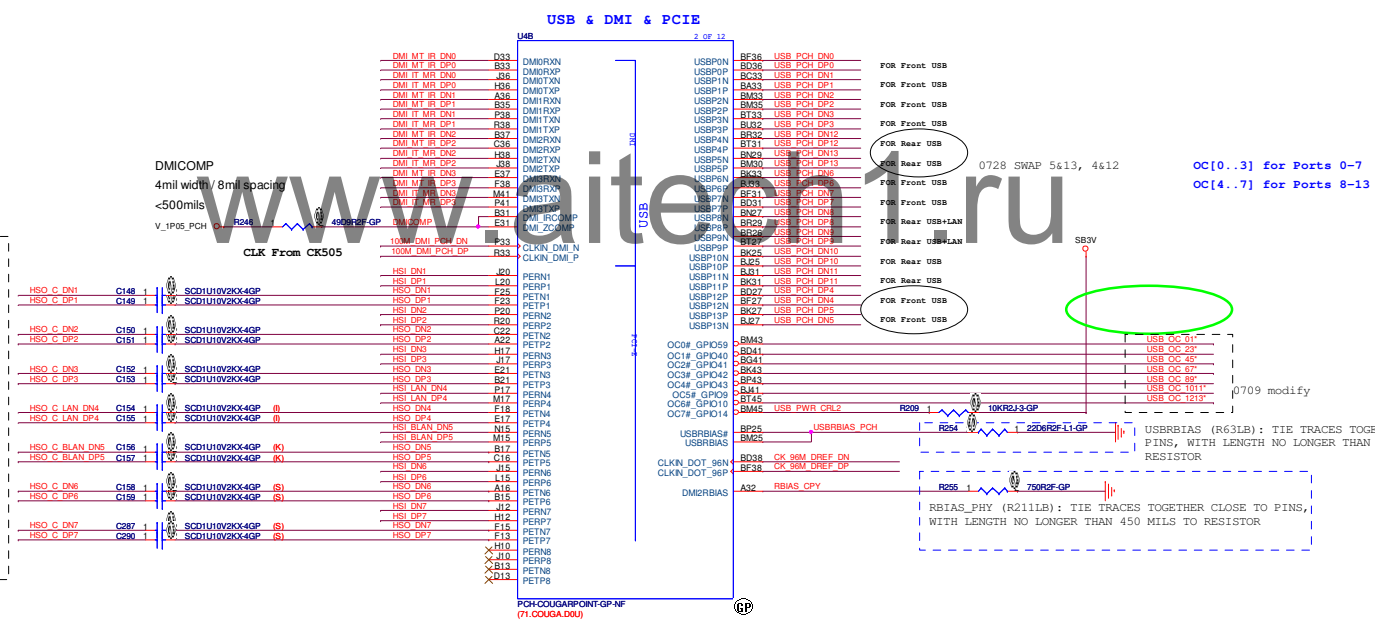
Size	Document Number
C	SERENA

Date: Thursday, September 02, 2010

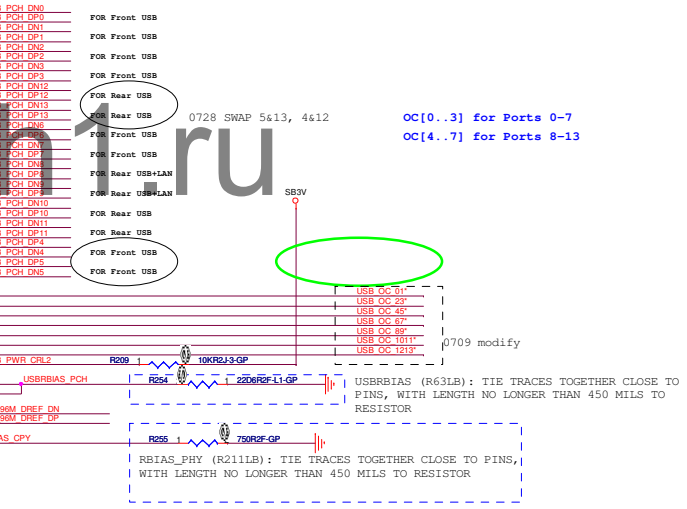
Sheet 20 of 51



PLACE NEAR PCI SLOT



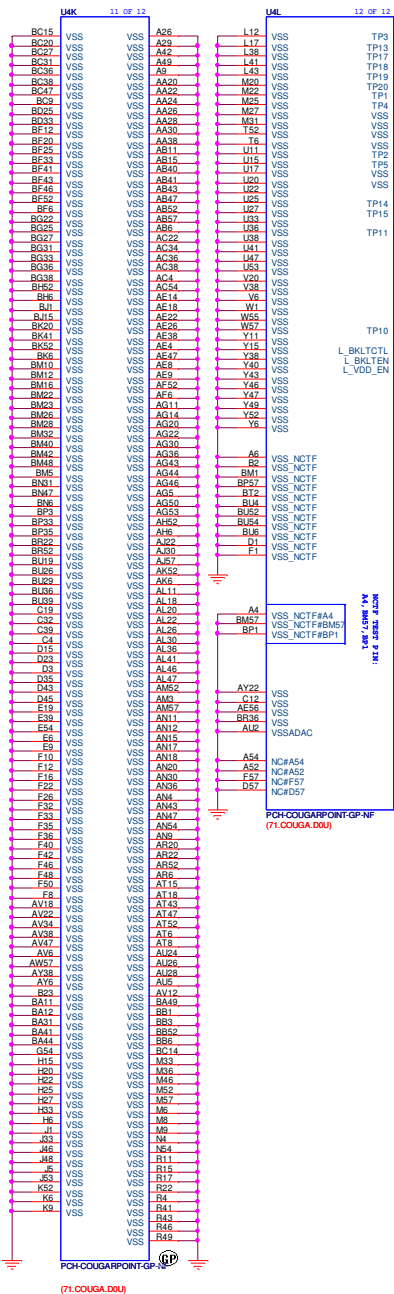
Place Near LAN Area



STRAP

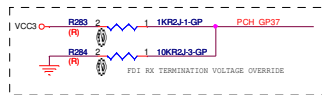
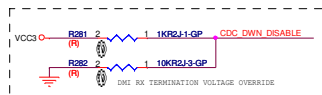
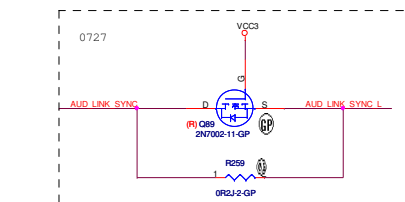
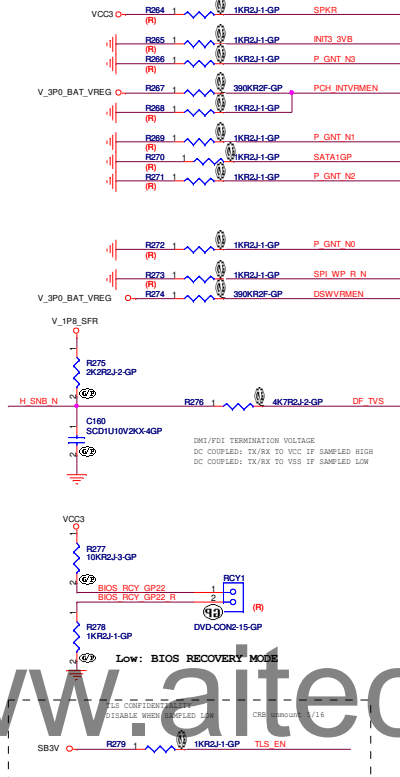
19 SPKR >>>
21 INIT3_3VB <<<
22 P_GNT_N3 <<<
19 PCH_INTVRMEN <<<
22 P_GNT_N2 <<<
22 P_GNT_N1 <<<
20 DF_TVS <<<
19 TLS_EN >>>
19 SPI_WP_R_N >>>
19 AUD_LINK_SYNC_R <<<
34 AUD_LINK_SYNC_L <<<
19 AUD_LINK_SYNC <<<
21 SATA1GP <<<
21 BIOS_RCY_GP22 <<<
10 H_SNB_N <<<
19 DSWVRMEN <<<
21 CDC_DWN_DISABLE <<<
21 PCH_GP37 <<<

BOARD ID



PCH COUGARPOINT GP NF
(71.00UGA.D00)

6' serial strapping define



BOOT DEVICE	GNT1	SATA1GP_GPIO19
SPKR	1	1
PCI	1	0
FWH	0	0

PCH Functional Straps

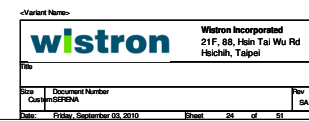
PCH EDS, Page 89, Table 89-93

SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).
INIT3_3VB	This signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low
P_GNT_N3	Top-Block Swap Override The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode
PCH_INTVRMEN	Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high
P_GNT_N1	Boot BIOS Destination Selection Signal has weak internal pull-ups.
SATA1GP (GPIO19)	Boot BIOS Destination Selection Signal has weak internal pull-ups.
P_GNT_N2	The signal has a weak internal pull-up.
AUD_LINK_SDO_R	Flash Descriptor Security Override Strap . The signal has a weak internal pull-down.
AUD_LINK_SYNC-R	On-Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
PCH_GP28_PU (GPIO28)	The signal has a weak internal pull-up. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
DF_TVS	DMI and FDI Tx/Rx Termination Voltage The signal has a weak internal pull-down.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
CDC_DWN_DISABLE (SATA2GP/GPIO36)	DMI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal pull-down
PCH_GP37 (SATA3GP/GPIO37)	FDI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal pull-down
TLS_EN (GPIO15)	The signal has a weak internal pull-down. Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality A strong pull up may be needed for GPIO functionality This signal must be pulled up to support Intel RPAAT and Intel AMT with TLS. Intel ME configuration parameters also need to be set correctly to enable TLS.

<Variant Name>

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Title	PCH GPIO/STRAPS
Size	Document Number
C	SEIENNA
Date	Thursday, September 02, 2010
Sheet	23 of 51



PCI

PCIEX16

11 EXP_A_RX_DN[0..15]
11 EXP_A_RX_DP[0..15]
11 EXP_A_TX_DP[0..15]
11 EXP_A_TX_DN[0..15]
20 CK_PE_100M_16PORT_DP
20 CK_PE_100M_16PORT_DN
26,40 PLTRST_SL_N

PCIEX1

MINI CARD

OTHERS

19,26,40 SMB_CLK_RESUME
19,26,40 SMB_DATA_RESUME

19,26,33,36 WAKE_N

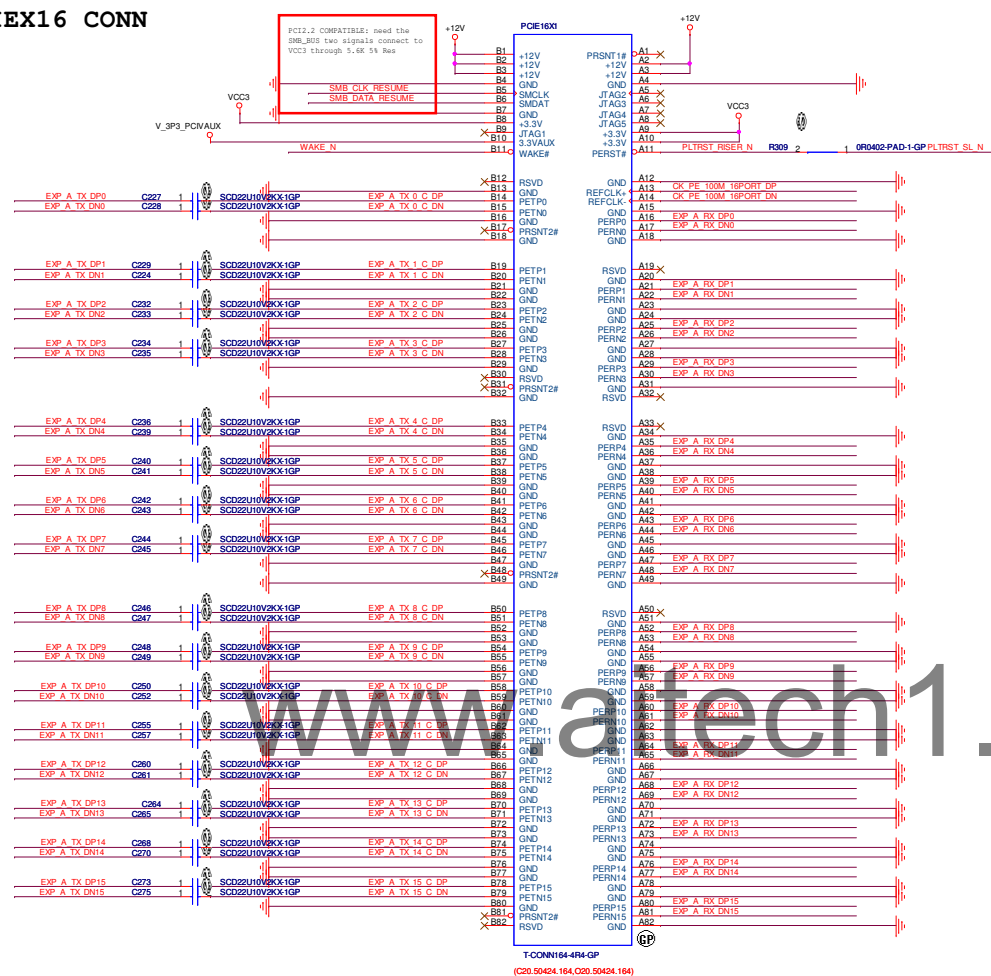
RISER ID

FAN

Thermal

Thermal Diode X1
FAN X1
PCI *2
MINI Card *2
PCI-E x1 *1
PCI-E x16 *1

PCIEX16 CONN



ONFI

PCIE1

22 HSI DN1
22 HSI DP1
22 HSO_C DN3
22 HSO_C DP3
20 OK_PCIE1_1_DN
20 OK_PCIE1_1_DP

PCIE1_2

22 HSI DN2
22 HSI DP2
22 HSO_C DN2
22 HSO_C DP2
20 OK_PCIE1_2_DN
20 OK_PCIE1_2_DP

PCIE1_3

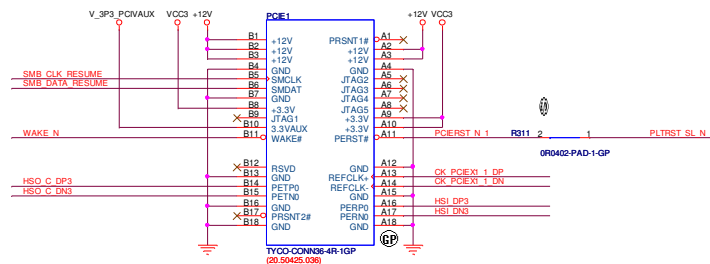
22 HSI DN1
22 HSI DP1
22 HSO_C DN1
22 HSO_C DP1
20 OK_PCIE1_3_DN
20 OK_PCIE1_3_DP

OTHER

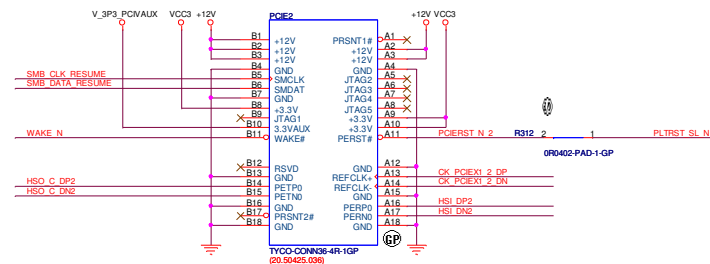
25,40 PLTRST_SL_N
19,25,40 SMB_CLK_RESUME
19,25,40 SMB_DATA_RESUME
19,25,33,36 WAKE_N

TPM

PCIE1 CONN



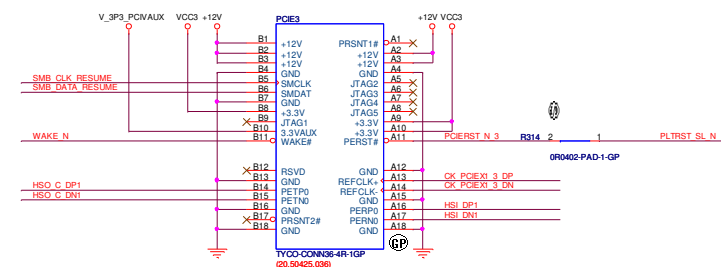
PCIE2 CONN



ONFI POWER

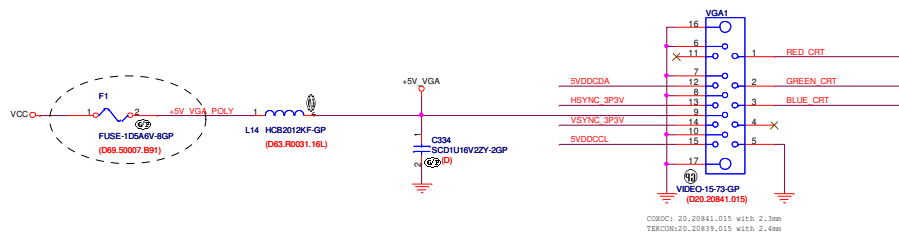
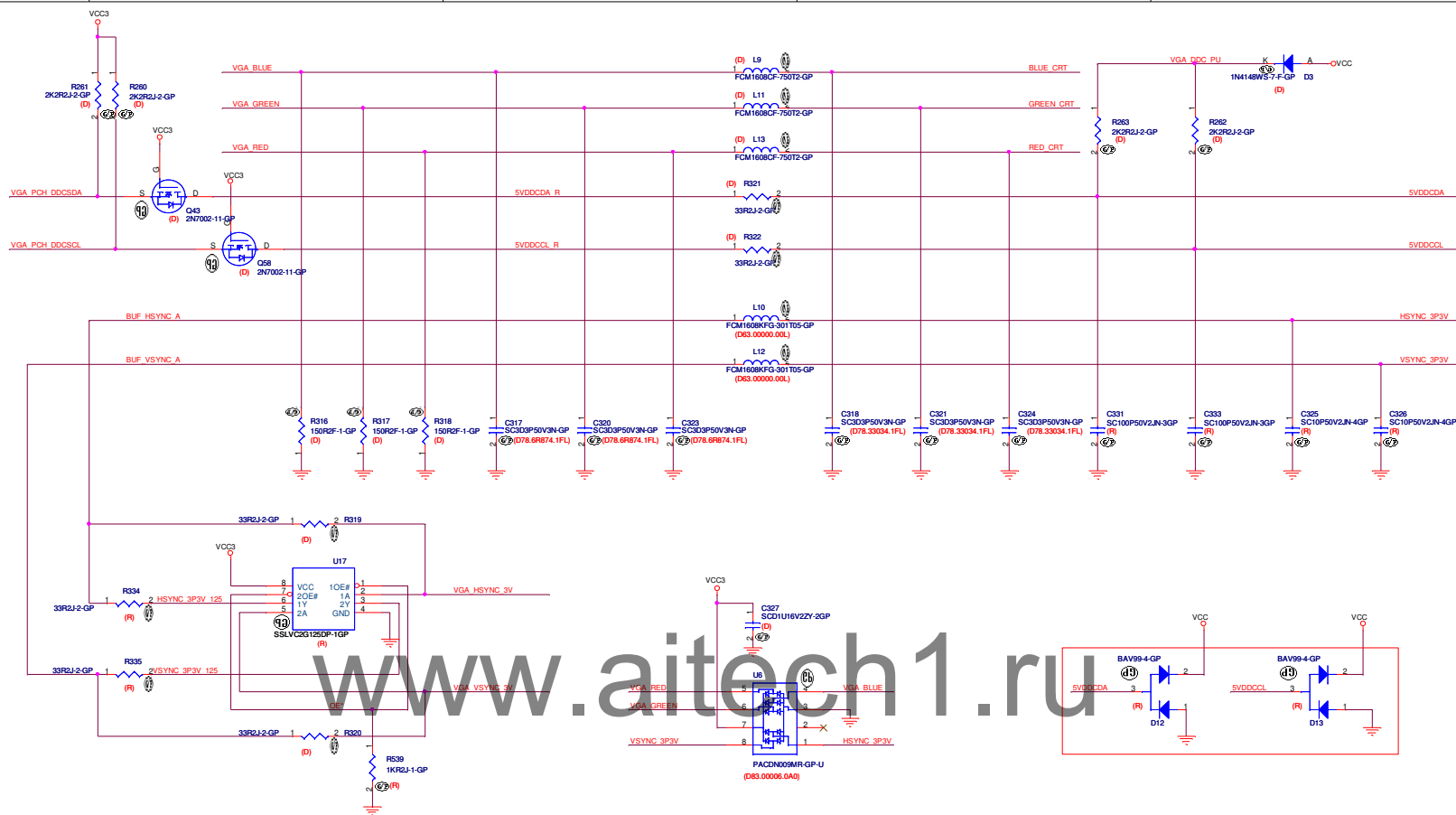
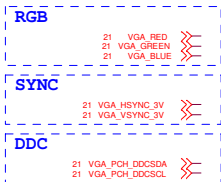
0713 Remove

PCIE3 CONN



TPM

0712 Remove

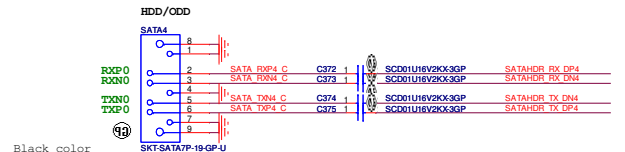
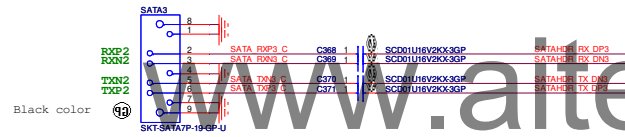
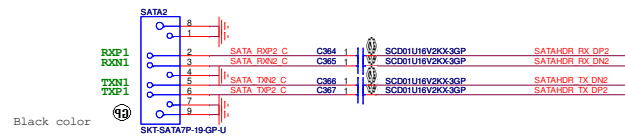
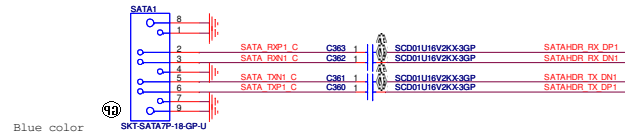
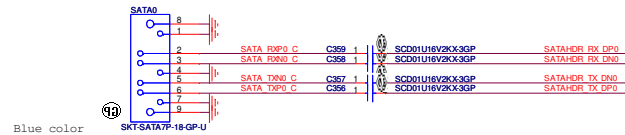


C00001: 20,20841,015 with 2.3mm
TERCON:20,20839,015 with 2.4mm

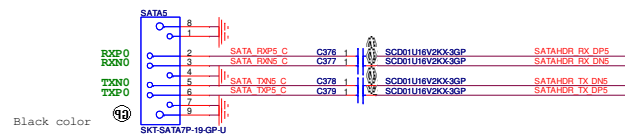


SATA

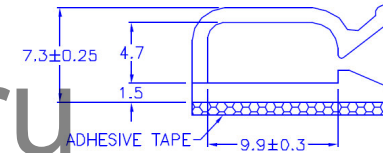
21	SATAHDR_RX_DP0	21	SATAHDR_RX_DN0
21	SATAHDR_TX_DN0	21	SATAHDR_TX_DP0
21	SATAHDR_RX_DP1	21	SATAHDR_RX_DN1
21	SATAHDR_TX_DN1	21	SATAHDR_TX_DP1
21	SATAHDR_RX_DP2	21	SATAHDR_RX_DN2
21	SATAHDR_TX_DN2	21	SATAHDR_TX_DP2
21	SATAHDR_RX_DP3	21	SATAHDR_RX_DN3
21	SATAHDR_TX_DN3	21	SATAHDR_TX_DP3
21	SATAHDR_RX_DP4	21	SATAHDR_RX_DN4
21	SATAHDR_TX_DN4	21	SATAHDR_TX_DP4
21	SATAHDR_RX_DP5	21	SATAHDR_RX_DN5
21	SATAHDR_TX_DN5	21	SATAHDR_TX_DP5



20.81111.007 Blue Lotes 20.81112.007 Black Lotes
 20.81201.007 Blue David 20.81200.007 Black David
 20.81054.007 Blue MOLEX 20.80618.007 Black MOLEX



Wire mount : 42.3P617.001



22	USB_PCH_DP0	↔
22	USB_PCH_DN0	↔
22	USB_PCH_DP1	↔
22	USB_PCH_DN1	↔
22	USB_PCH_DP2	↔
22	USB_PCH_DN2	↔
22	USB_PCH_DP3	↔
22	USB_PCH_DN3	↔
22	USB_OC_01*	↔
22	USB_OC_23*	↔
22	USB_PCH_DP6	↔
22	USB_PCH_DN6	↔
22	USB_PCH_DP7	↔
22	USB_PCH_DN7	↔
22	USB_PCH_DP12	↔
22	USB_PCH_DN12	↔
22	USB_PCH_DP13	↔
22	USB_PCH_DN13	↔
22	USB_OC_07*	↔
22	USB_OC_1213*	↔

5VDUAL_USB_F 0 1 2 VCC_USB_01 L USBVCC01

F3 POLYSW-2ABV-GP (69.50014.001)

USB_OC_01*

C381 SC1KP50V20K-1GP

R340 10KRJ2-3-GP

R341 15KRJ2-1-GP

C380 SCD1U16V22Y-2GP

5V

5VDUAL_USB_F 0 1 2 VCC_USB_23 L USBVCC23

F3 POLYSW-2ABV-GP (69.50014.001)

USB_OC_25*

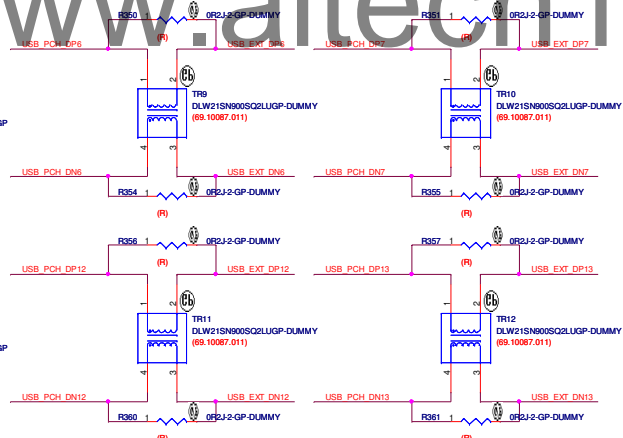
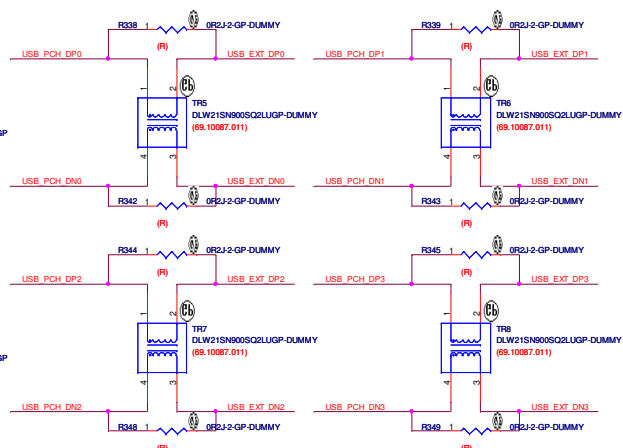
C383 SC1KP50V20K-1GP

R346 10KRJ2-3-GP

R347 15KRJ2-1-GP

C382 SCD1U16V22Y-2GP

5V



REAR USB

22 USB_PCH_DN10
22 USB_PCH_DP10
22 USB_PCH_DN11
22 USB_PCH_DP11

REAR USB+LAN

22 USB_PCH_DP8
22 USB_PCH_DN8
22 USB_PCH_DP9
22 USB_PCH_DN9

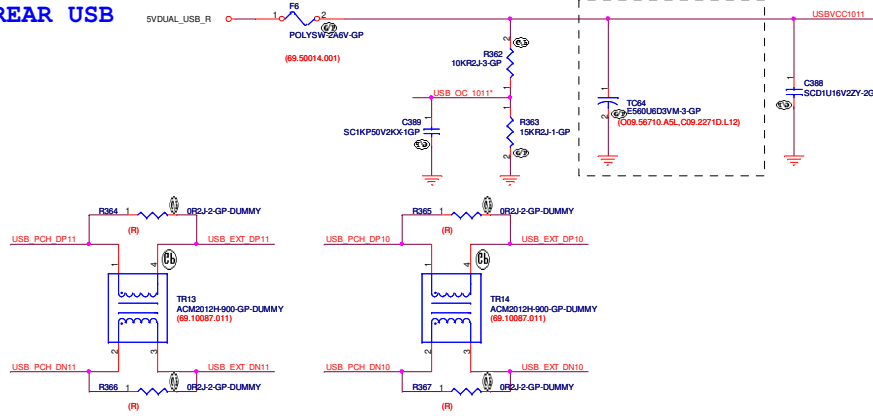
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22 USB_PCH_DP4
22 USB_PCH_DN4
22 USB_PCH_DP5
22 USB_PCH_DN5

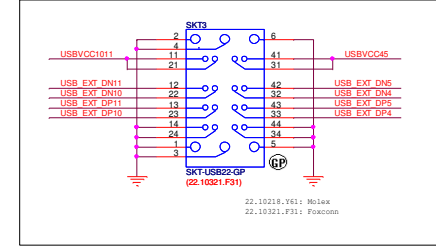
REAR USB

22 USB_OC_45*
22 USB_OC_99*
22 USB_OC_1011*

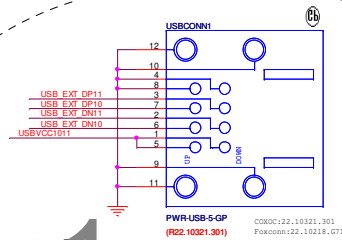
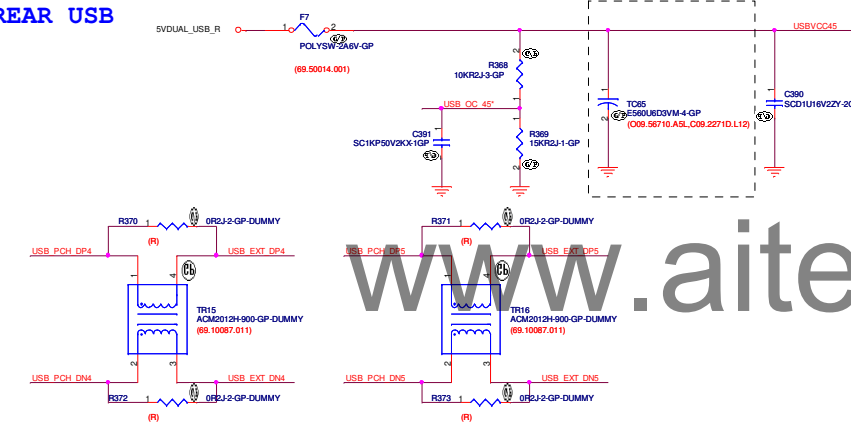
REAR USB



0827 SWAP port 4/5 and 10/11

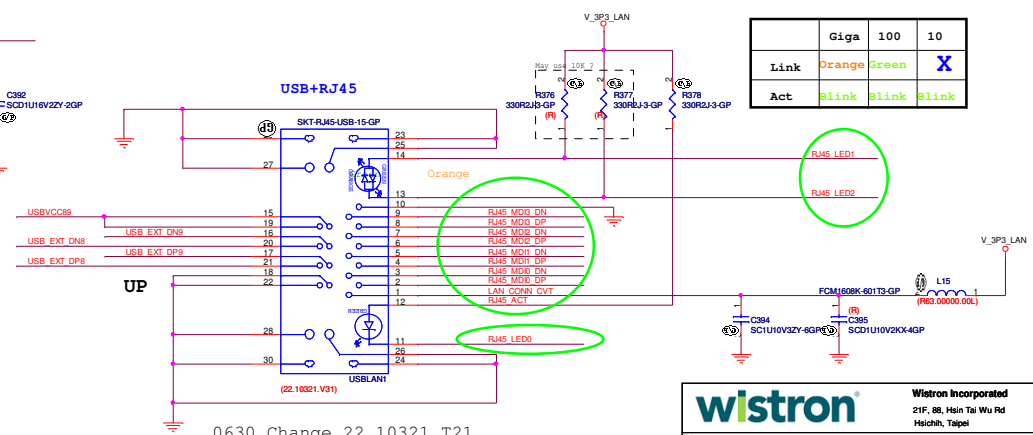
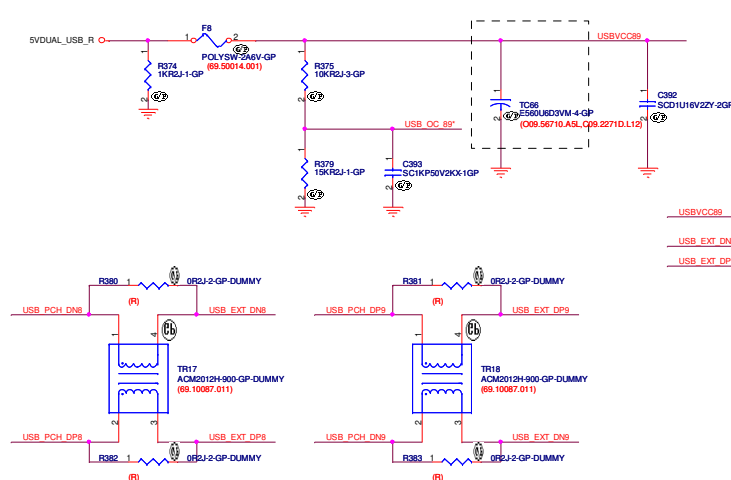


REAR USB



Co-layout

REAR USB+LAN

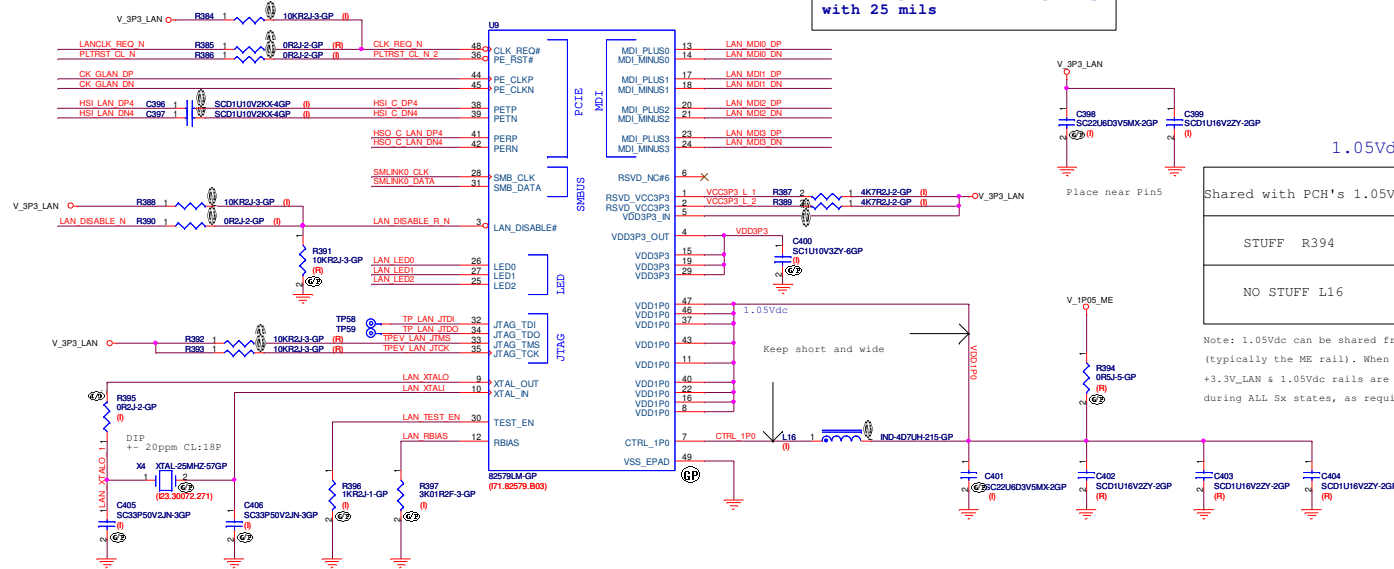


0630 Change 22.10321.T21

19 LANCLK_REQ_N <<
 20 CK_GLAN_DP <<
 20 CK_GLAN_DN <<
 22 HSI_LAN_DP4 <<
 22 HSI_LAN_DN4 <<
 22 HSO_C_LAN_DP4 <<
 22 HSO_C_LAN_DN4 <<
 19 SMLINK0_CLK <<
 19 SMLINK0_DATA <<
 33,36,40 PLTRST_CL_N <<
 19 LAN_DISABLE_N <<
 33 SPEED_1000_N <<
 33 SPEED_100_N <<
 33 LINK_ACTIVITY_N <<
 33 BLAN_TRON_0 <<
 33 BLAN_TRON_1 <<
 33 BLAN_TRON_2 <<
 33 BLAN_TRON_3 <<
 33 BLAN_TRON_4 <<
 31 RU45_MDIO_DP <<
 31 RU45_MDIO_DN <<
 31 RU45_MDIO_DP <<
 31 RU45_MDIO_DN <<
 31 RU45_MDIO_DP <<
 31 RU45_MDIO_DN <<
 31 RU45_MDIO_DP <<
 31 RU45_MDIO_DN <<
 31,44 RU45_LED0 <<
 31 RU45_LED1 <<
 31 RU45_LED2 <<

If CLK_REQ_N is connected
 to PCIeCLKRQ[1:2]#, the
 CLK_REQ_N pull-up resistor
 should be connected to +V3.3S.

LAN_MDI_P / LAN_MDI_N
 routing guide line: 4 mils on
 10 mils spacing
 Pair to pair should keep away
 with 25 mils

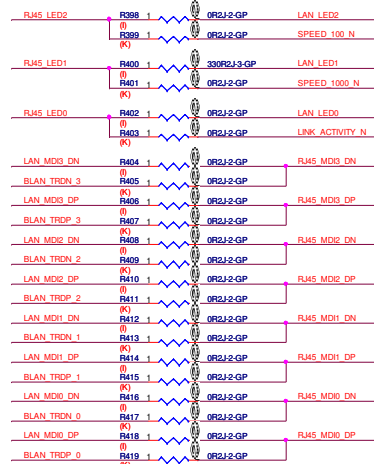


1.05Vdc POWER OPTIONS

Shared with PCH's 1.05V SVR	Internal SRV
STUFF R394	STUFF L16
NO STUFF L16	NO STUFF R394

Note: 1.05Vdc can be shared from PCH's 1.05V SVR
 (typically the ME rail). When sharing, make sure both
 +3.3V_LAN & 1.05Vdc rails are remained powered on
 during ALL Sx states, as required to support WOL.

www.aitech1.ru
 Realtek LAN: C, L, T series (K)
 Intel LAN: J, D series (I)



HD_LINK

19 AUD_LINK_SDR
19 AUD_LINK_SDO
19.35 AUD_LINK_RST_N
23 AUD_LINK_SYNC_L
19 AUD_LINK_BCLK

AUDIO PORT

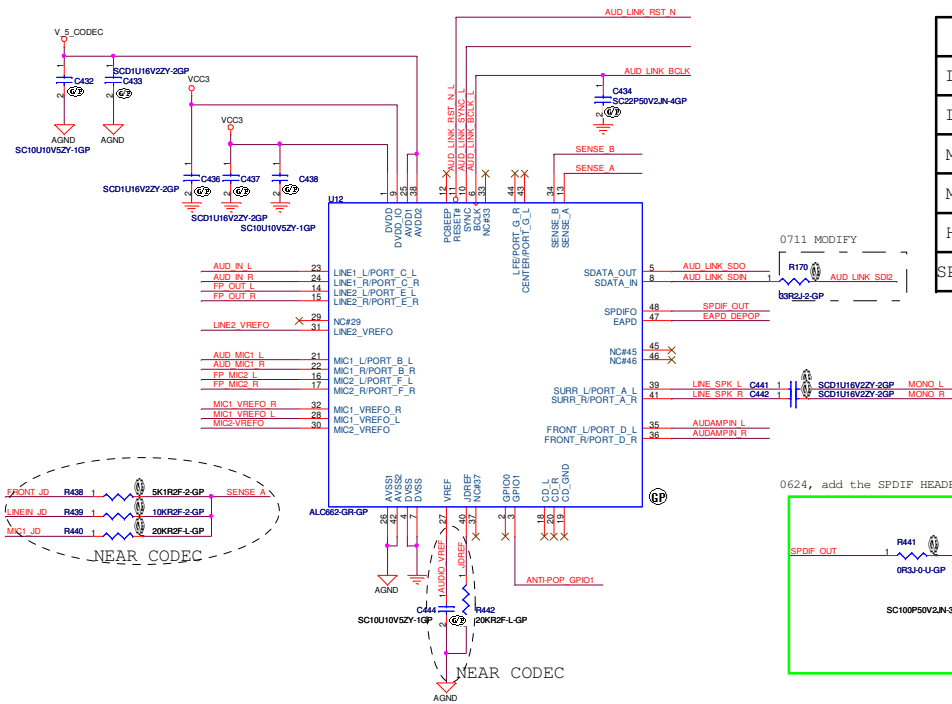
35 AUD_IN_L
35 AUD_IN_R
35 AUD_MIC1_L
35 AUD_MIC1_R
35 MIC1_VREF0_R
35 MIC1_VREF0_L
35 AUDAMPIN_L
35 AUDAMPIN_R
35 MIC2_LL
35 MIC2_RR
35 FP_OUTL_LL
35 FP_OUTL_RR
19 FP_AUD_DETECT

MISC

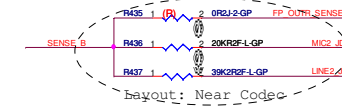
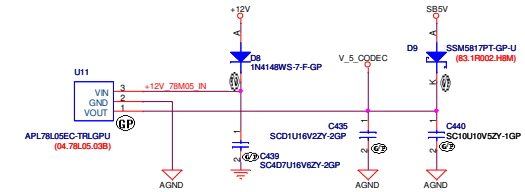
35 FRONT_ID
35 LINEIN_ID
35 MIC1_ID
35 MUTE
35 EAPD_DEPOP

GPIO

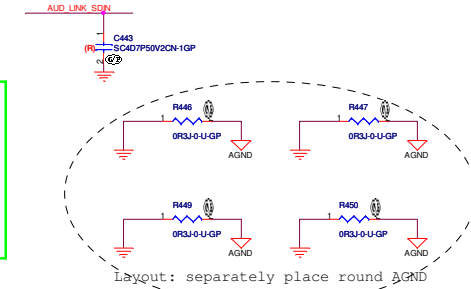
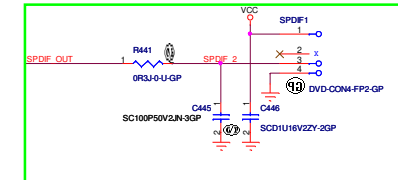
35 ANTI_POP_GP101



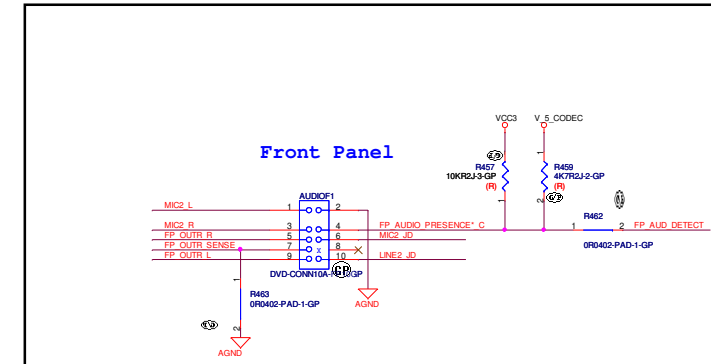
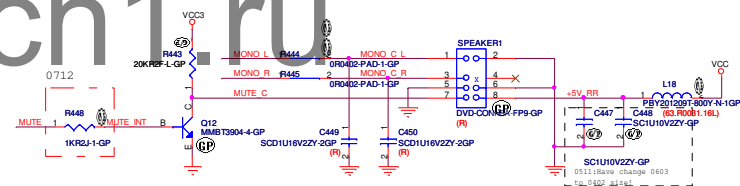
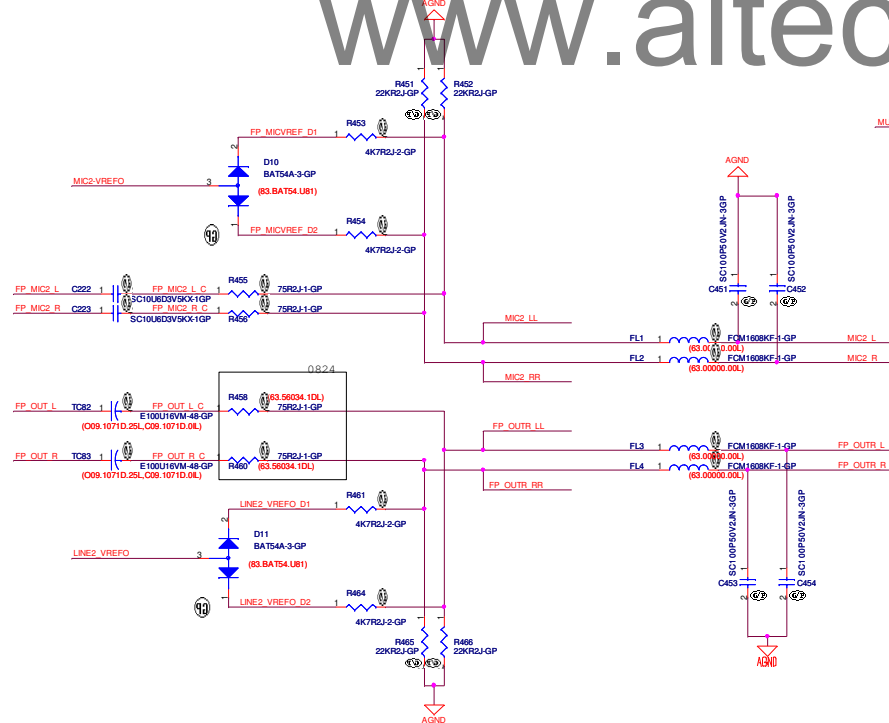
	ALC888S
Line-in	pin23/24
Line-out	pin35/36
Mic-in 1	pin21/22
Mic-in 2	pin16/17
HP-out	pin14/15
SPDIF-out	pin48



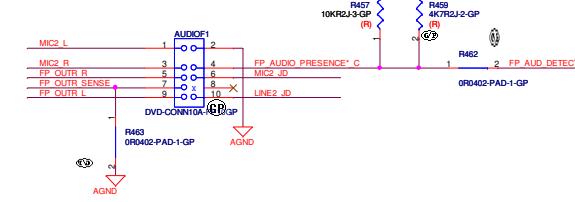
0624, add the SPDIF HEADER function



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Front Panel



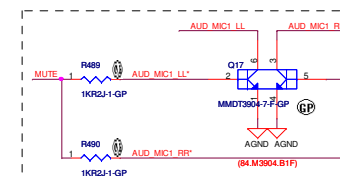
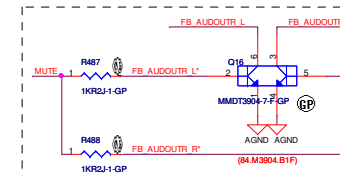
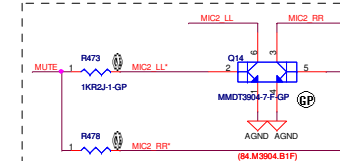
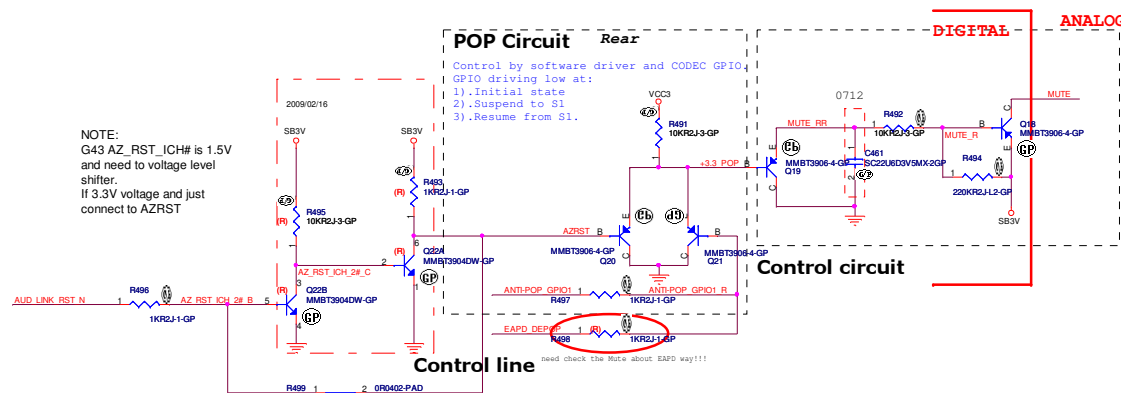
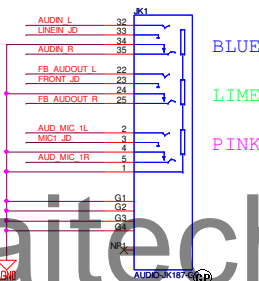
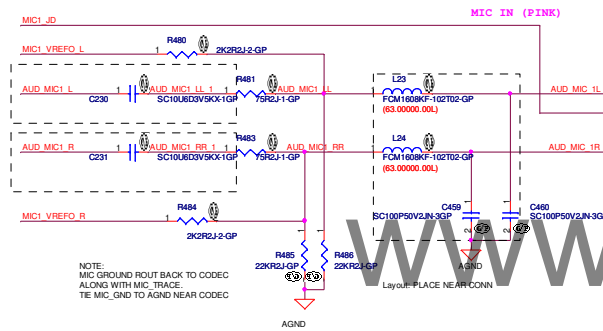
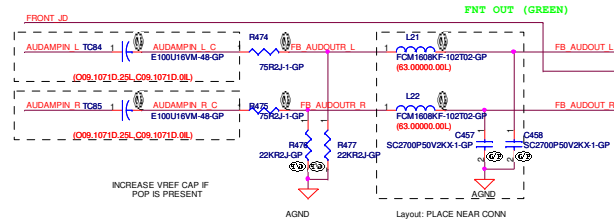
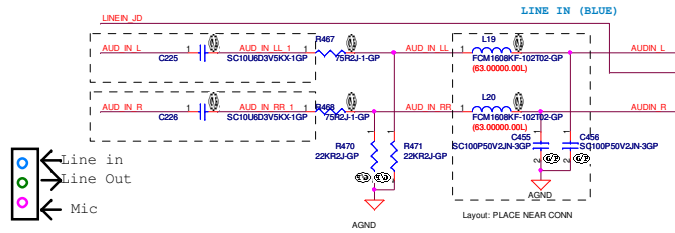
34	FP_OUTR_LL	⌘
34	FP_OUTR_RR	⌘
34	MIC2_LL	⌘
34	MIC2_RR	⌘
34	AUD_IN_L	⌘
34	AUD_IN_R	⌘
34	MIC1_VREFO_L	⌘
34	AUD_MIC1_L	⌘
34	AUD_MIC1_R	⌘
34	MIC1_VREFO_R	⌘
34	AUDAMPIN_L	⌘
34	AUDAMPIN_R	⌘

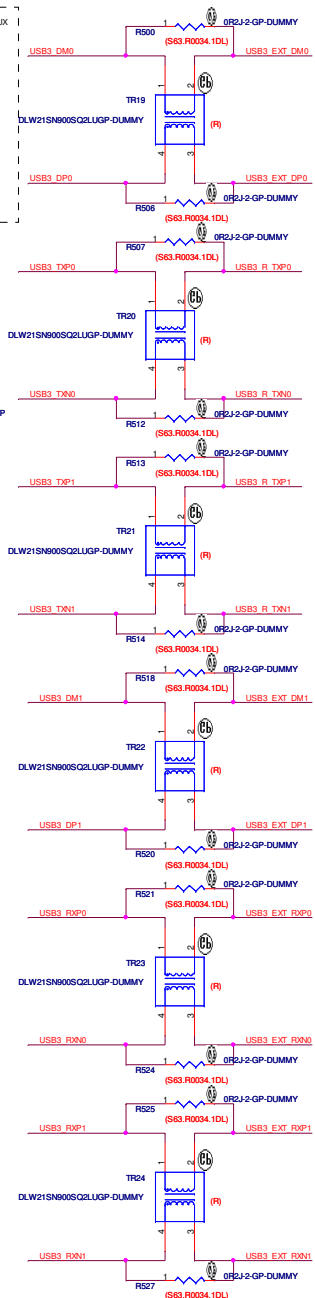
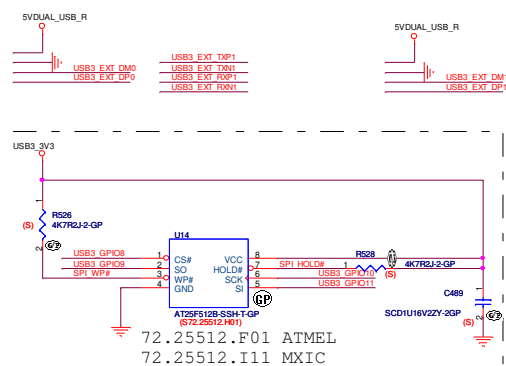
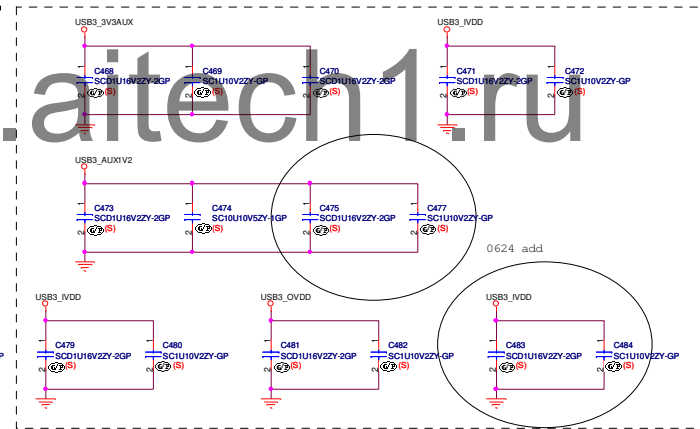
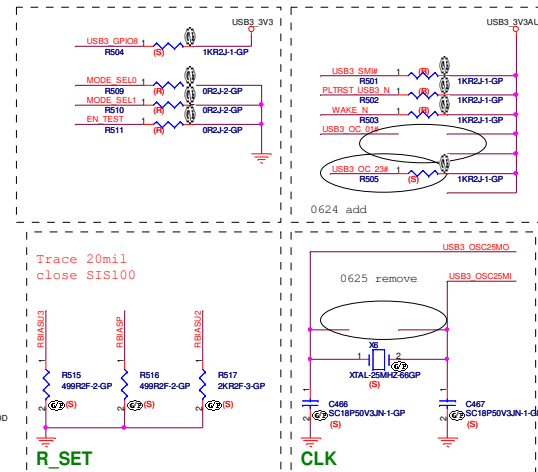
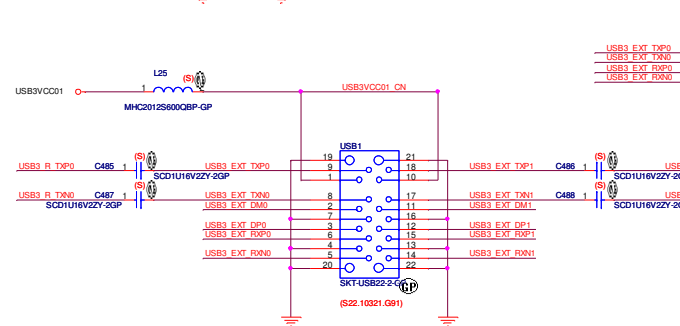
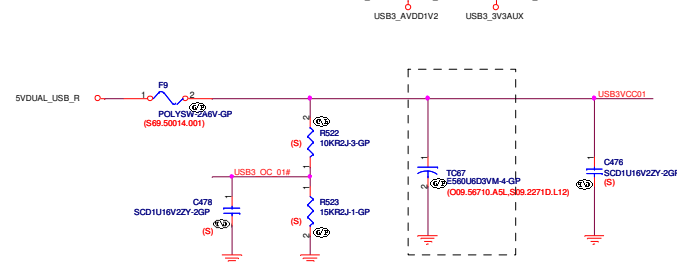
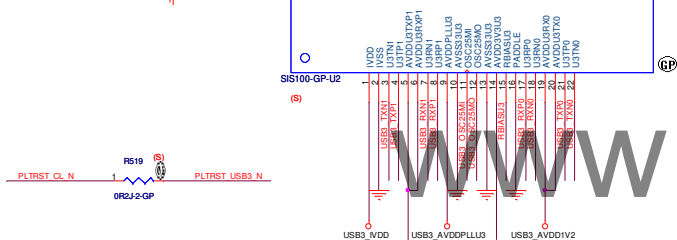
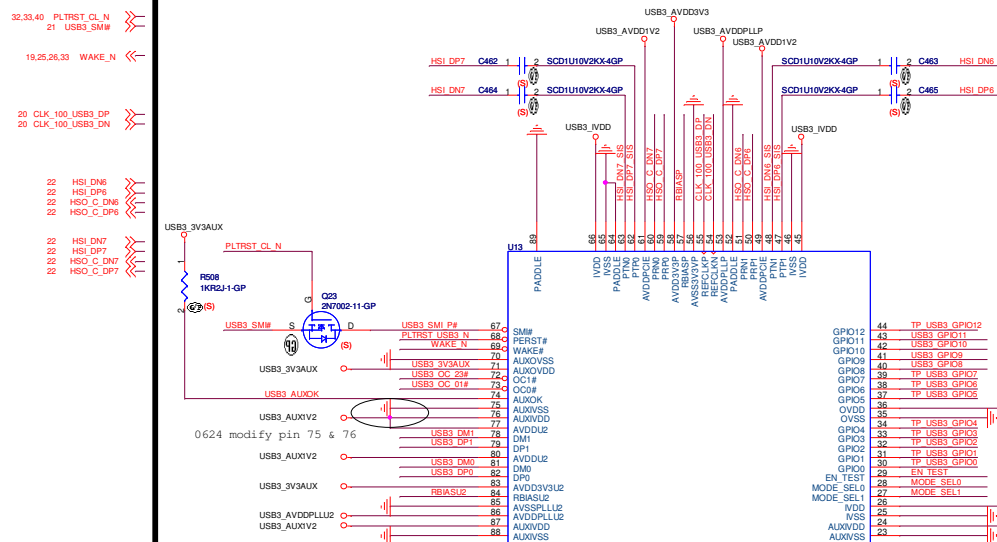
```

34  LINE1_JD  <<-----
34  FRONT_JD  <<-----
34  MIC1_JD   <<-----

9,34 AUD_LINK_RST_N >>-----
34  ANTI-POP_GPIO1 >>-----
34  EAPD_DEPOP >>-----
34  MUTE <<-----

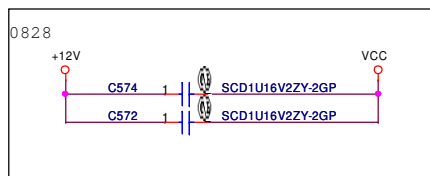
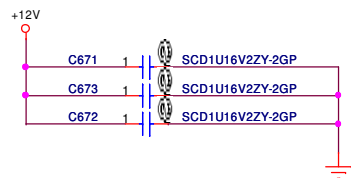
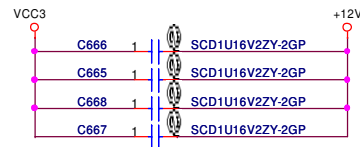
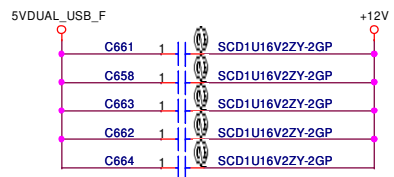
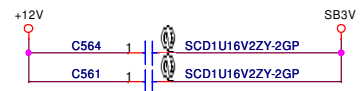
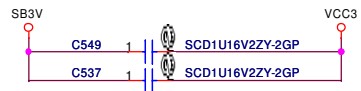
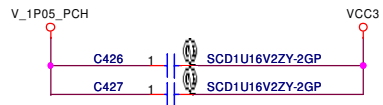
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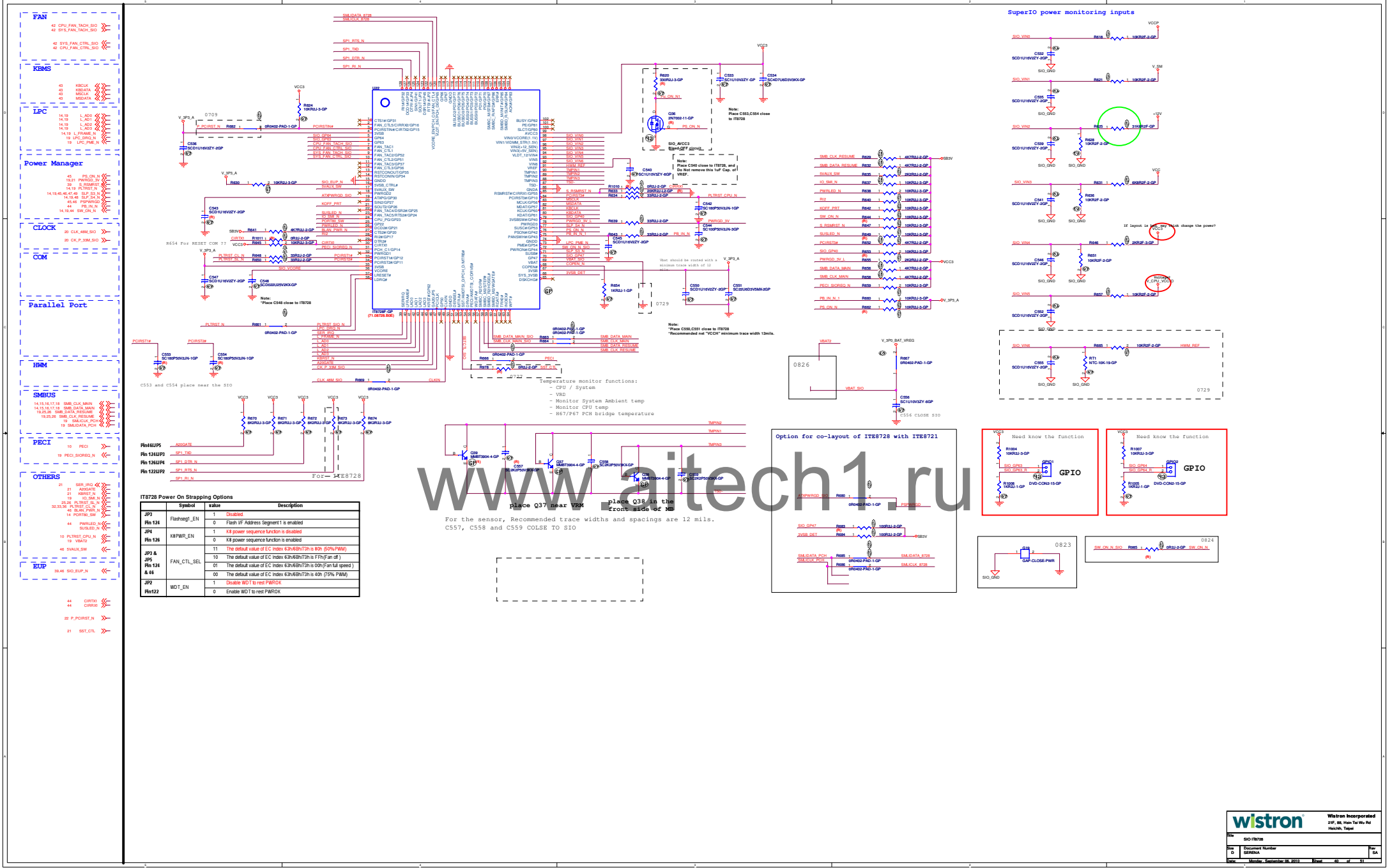




0708
0717 DEL



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IT8728 Power On Strapping Options

Symbol	value	Description
JP1	Flashwrt_EN	0 Flash IP Address Segment 1 is enabled
Pin 124	JP4	1 K8 power sequence function is disabled
Pin 126	K8PWR_EN	0 K8 power sequence function is enabled
JP3 & JP5	FAN_CTL_SEL	11 The default value of EC Index 63h/68h/72h is 60h (50% PWM)
Pin 124	6-6h	10 The default value of EC Index 63h/68h/72h is FFh (fan off)
6-6h	01	The default value of EC Index 63h/68h/72h is 00h (fan full speed)
JP2	WDT_EN	00 The default value of EC Index 63h/68h/72h is 40h (75% PWM)
Pin 122	WDT_EN	0 Enable WDT to reset PWR0K

For the sensor, Recommended trace widths and spacings are 12 mils.
C557, C558 and C559 COLSE to SIO

PARALLEL PORT

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SERIAL CONNECTER

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title TBD			
Size C	Document Number SERENA		Rev SA
Date:	Sunday, July 11, 2010	Sheet	41 of 52

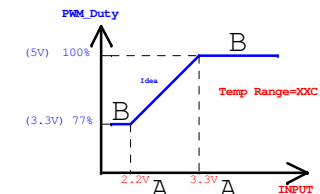
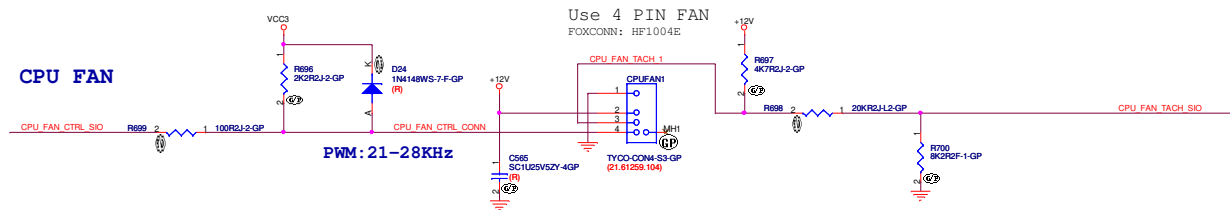
CPU FAN

40 CPU_FAN_TACH_SIO <<-
40 CPU_FAN_CTRL_SIO >>-

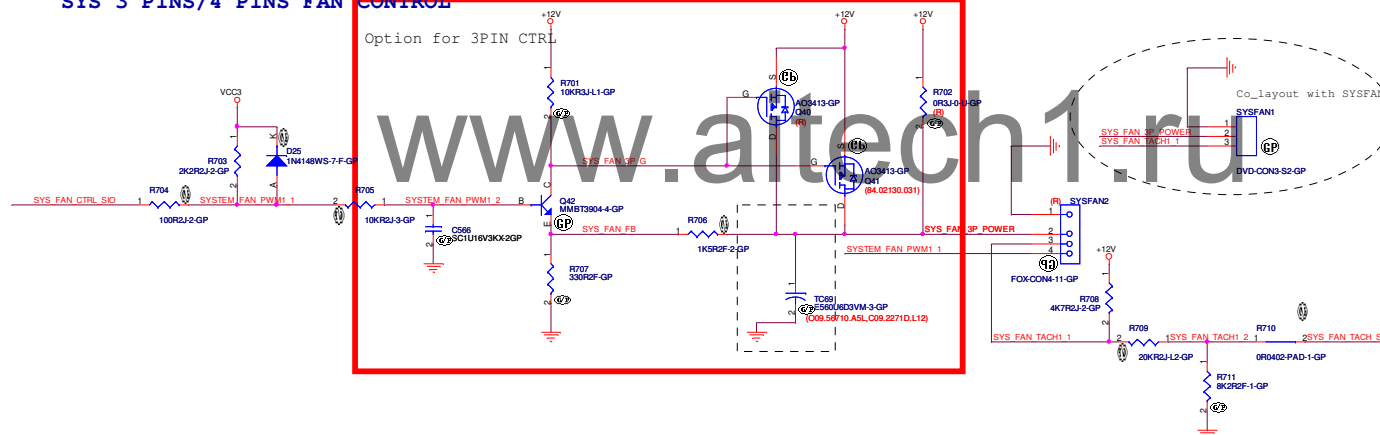
PSU FAN

SYS FAN

40 SYS_FAN_TACH_SIO <<-
40 SYS_FAN_CTRL_SIO >>-



SYS 3 PINS/4 PINS FAN CONTROL



AMT

TPM

close to TPM chip

```

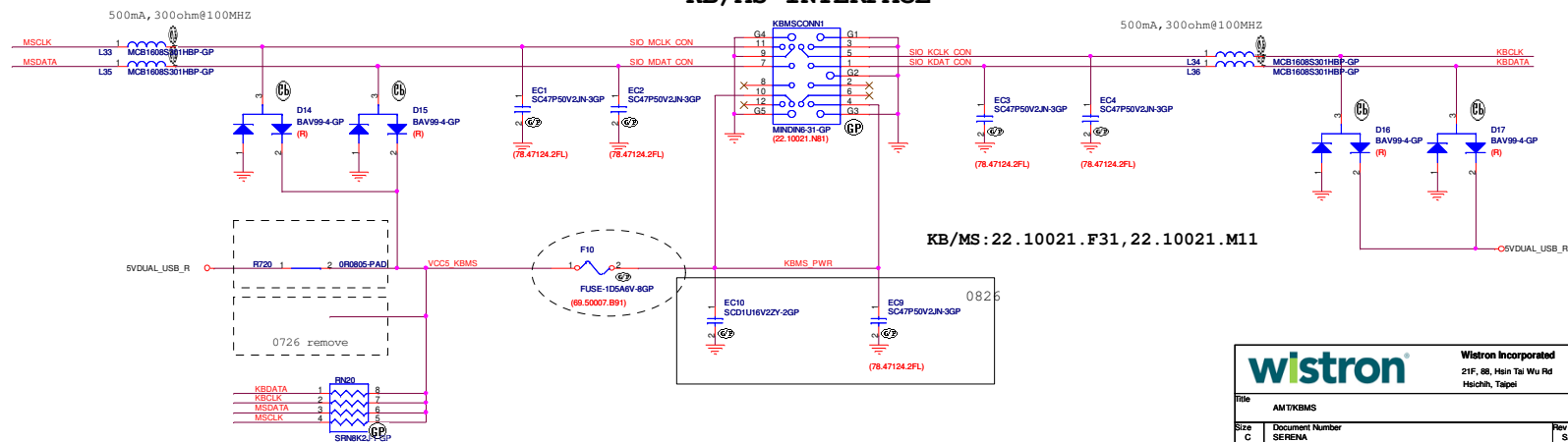
Reserve for TPM function debug

```

FOR flash Descriptor Security

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KB/MS INTERFACE



SUS LED

40 SUSLED_N >>

PWR LED

40 PWRLED_N >>

HDD LED

21 PCH_SATA_LED_N >>

OTHERS

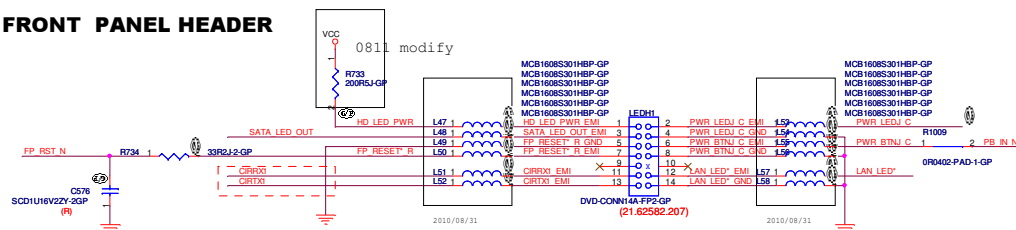
40 PB_IN_N <<

14,19,40,48 SLP_S4_N >>

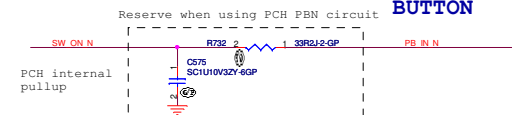
14,19,40 SW_ON_N <<

0826

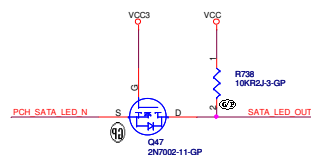
FRONT PANEL HEADER



POWER BUTTON



HDD LED



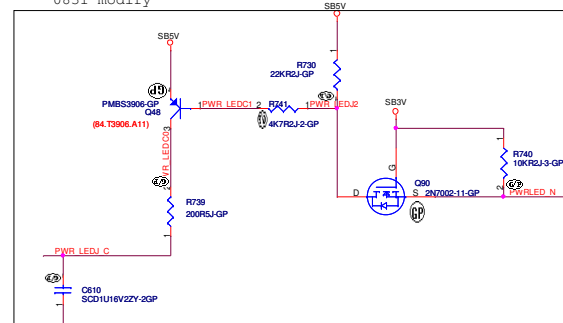
POWER LED

POWER BUTTON

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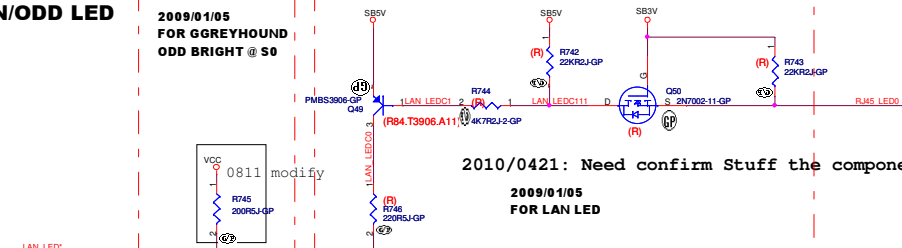
BIOS: Open Gain.
Default High.VCCH

0831 modify



LAN/ODD LED

2009/01/05
FOR GGREYHOUND
ODD BRIGHT @ 50

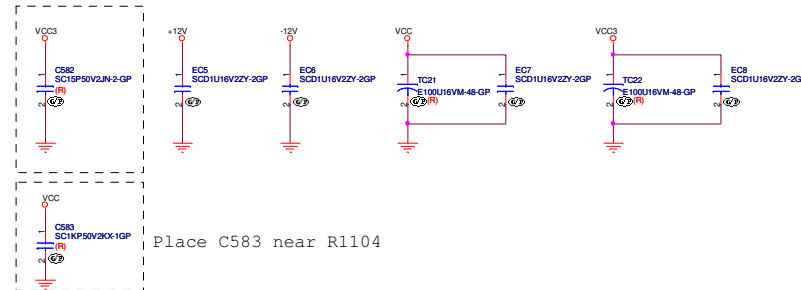
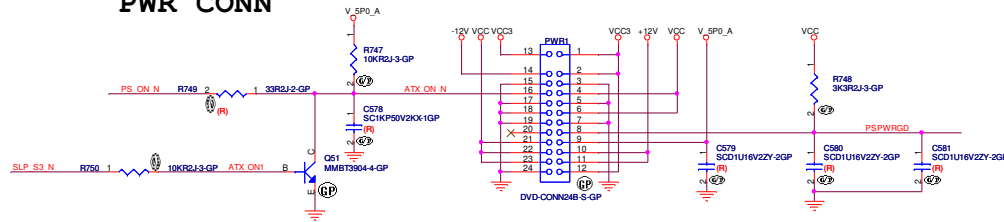


2010/0421: Need confirm Stuff the components or not !!!!

2009/01/05
FOR LAN LED

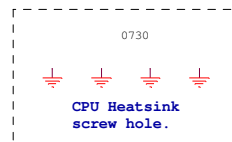
wistron		Wistron Incorporated	
12F, 88, Hsin Tai Wu Rd		Haichih, Taipei	
Title		SW LED / FRONT Panel	
Size		Document Number	
C		SERENA	
Date:		Monday, September 08, 2010	
Sheet		44 of 51	

PWR CONN

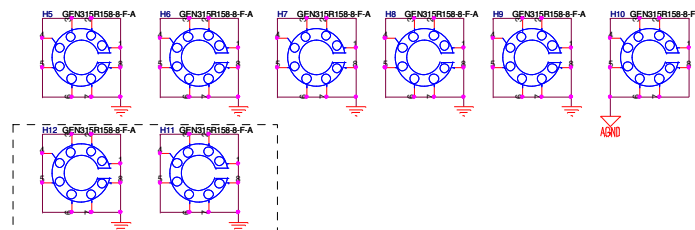


Place C583 near R1104

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CPU Heatsink Mylar

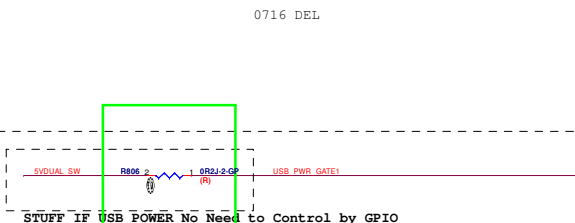
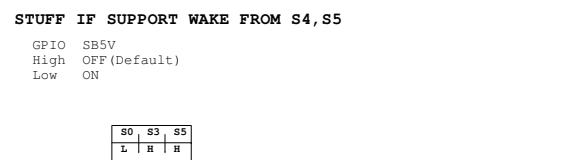
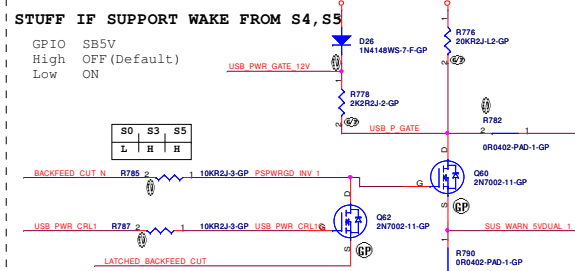
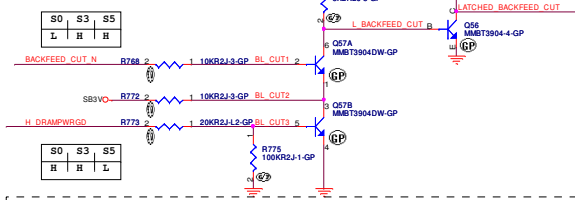
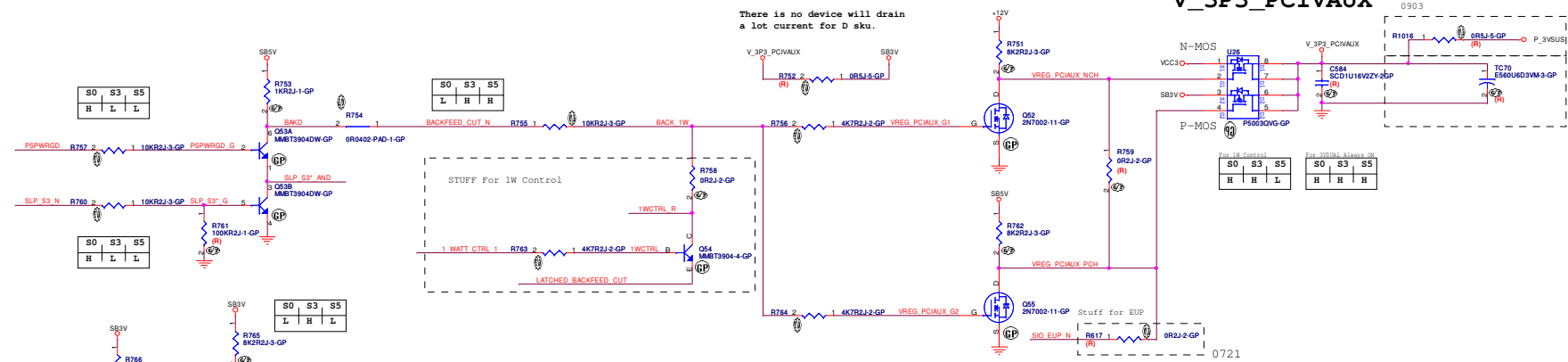


Dual Power Control

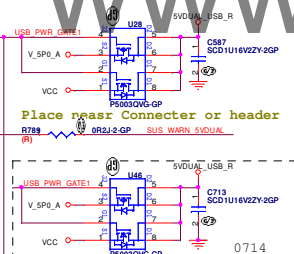
40.45 PSPWRGD >>
14.19.40.45.47.49 SLP_S3_N >>
19 1_WATT_CTRL_1 >>
19 SLP_LAN_N >>
14.19.47 PCH_SLP_A >>

40 SVAUX_SW >>
19 H_DRAMPWRGD >>
19 USB_PWR_CRL1 >>
22 USB_PWR_CRL2 >>
40 BLAN_PWR_N >>
39 SUS_WARN_SVDUAL >>

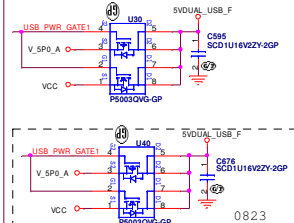
39.40 SIO_EUP_N >>



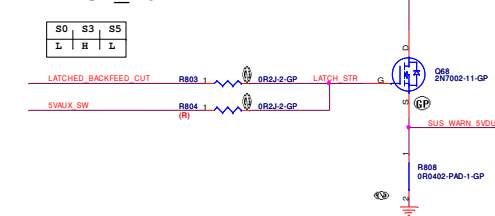
Rear USB PWR



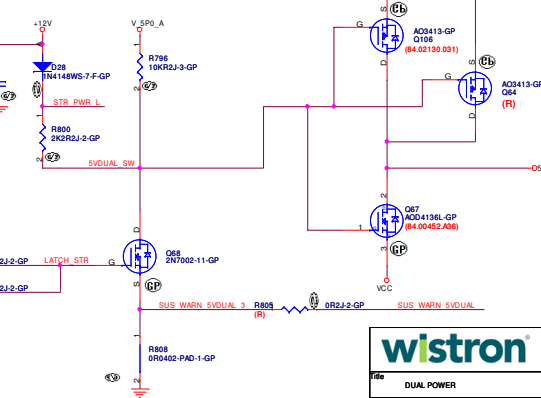
Front USB PWR

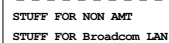
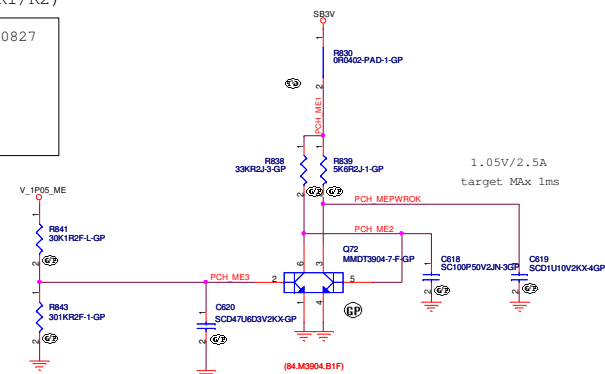
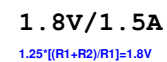
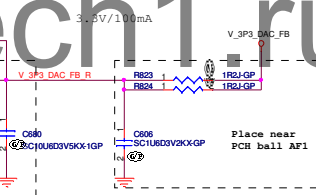
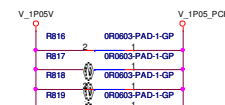


DIMM 5V_DUAL



DIMM 5V_DUAL

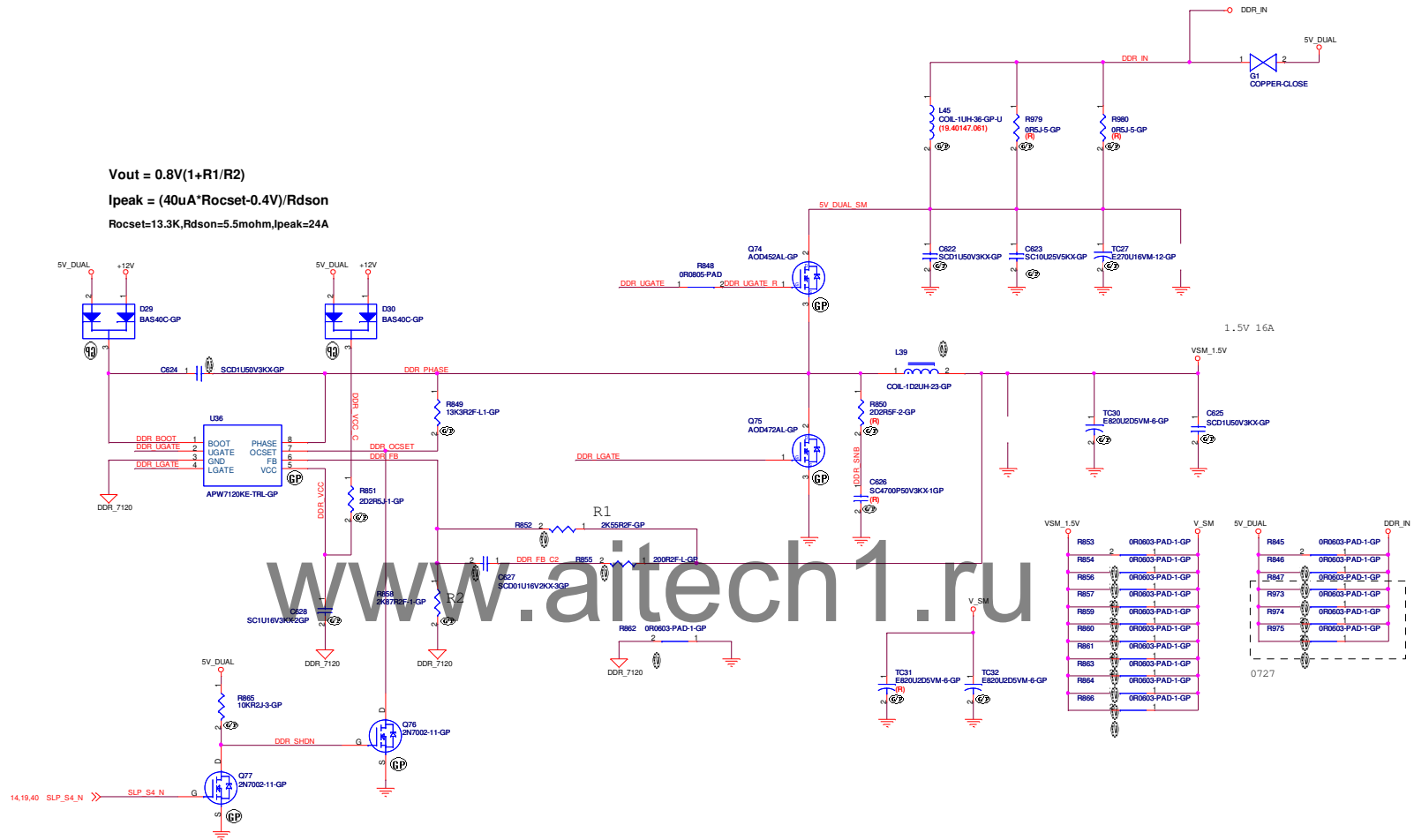




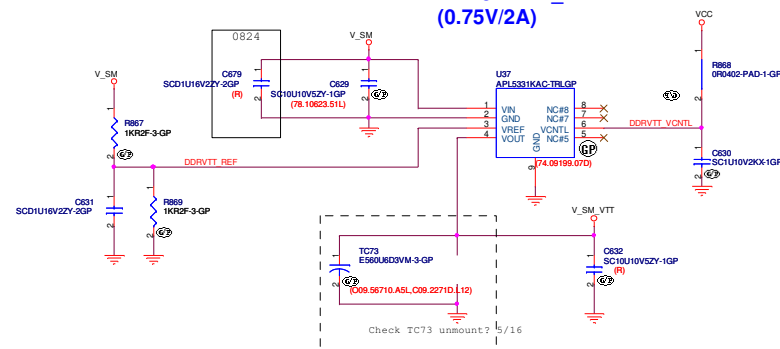
$$V_{out} = 0.8V(1+R1/R2)$$

$$I_{peak} = (40\mu A \cdot R_{ocset} - 0.4V) / R_{dson}$$

$$R_{ocset} = 13.3K, R_{dson} = 5.5m\Omega, I_{peak} = 24A$$



DDR3 MEM_VTT (0.75V/2A)



PCH

CPU SA POWER

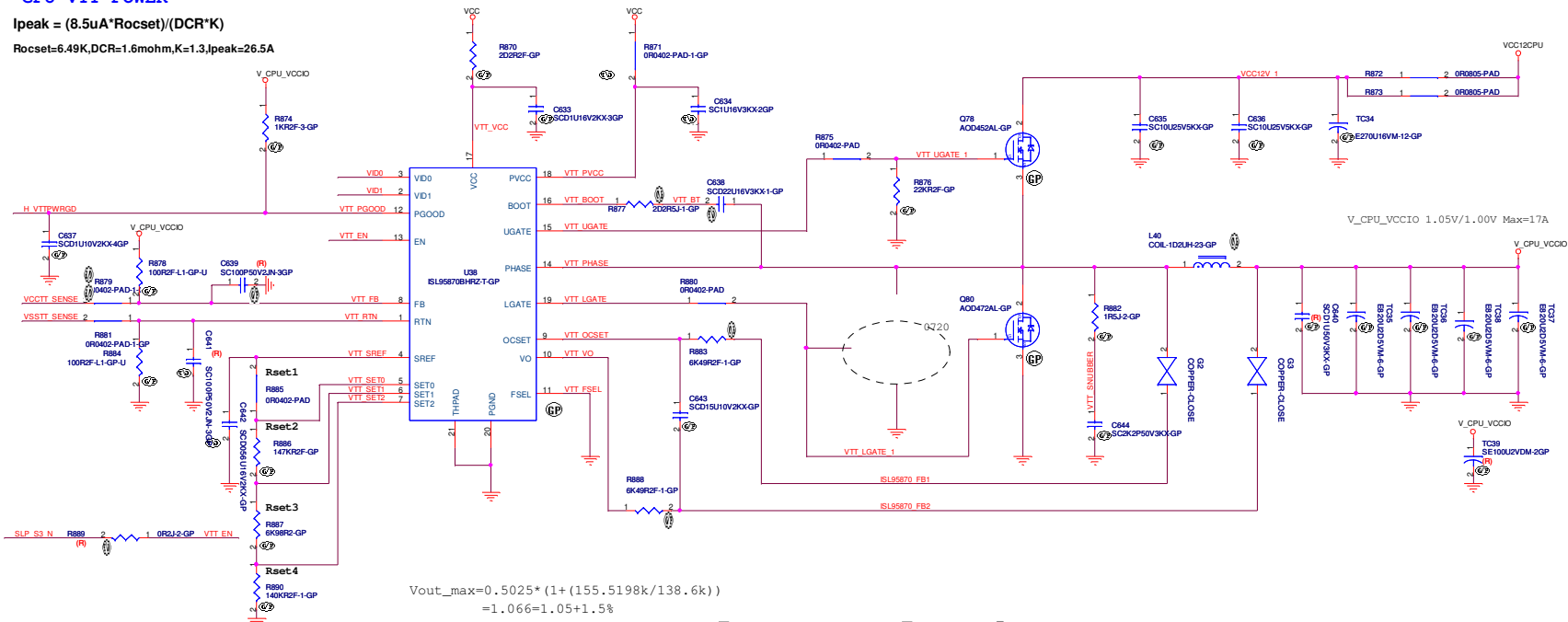
```

10  VCCSA_VID >>>
10  VCCSA_SENSE <<<

```

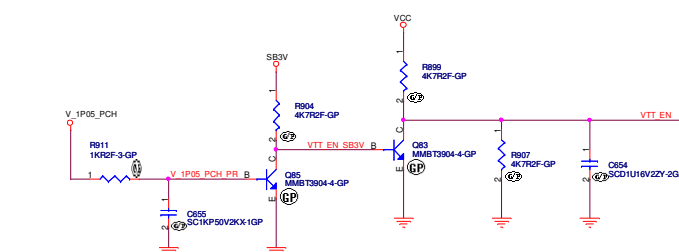
$$I_{peak} = (8.5\mu A * R_{ocset}) / (DCR * K)$$

Rocset=6.49K,DCR=1.6mohm,K=1.3,Ipeak=26.5A

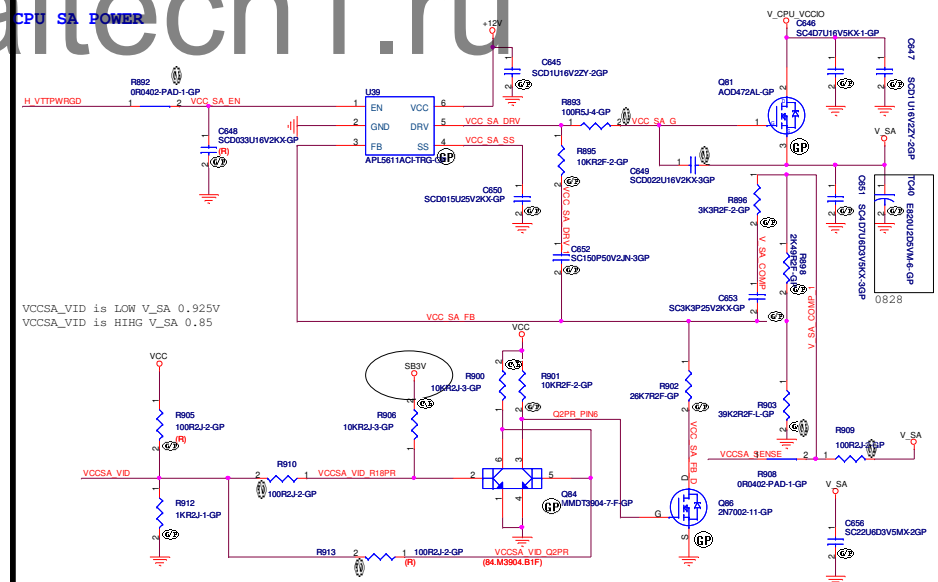


VID0	VID1	Vout
1	0	1.0V
0	0	1.05V

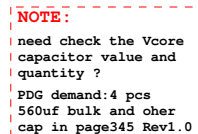
VCCIO_SEL	Voltage
1	1.05
0	1.00



CPU SA POWER



VCC CORE



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